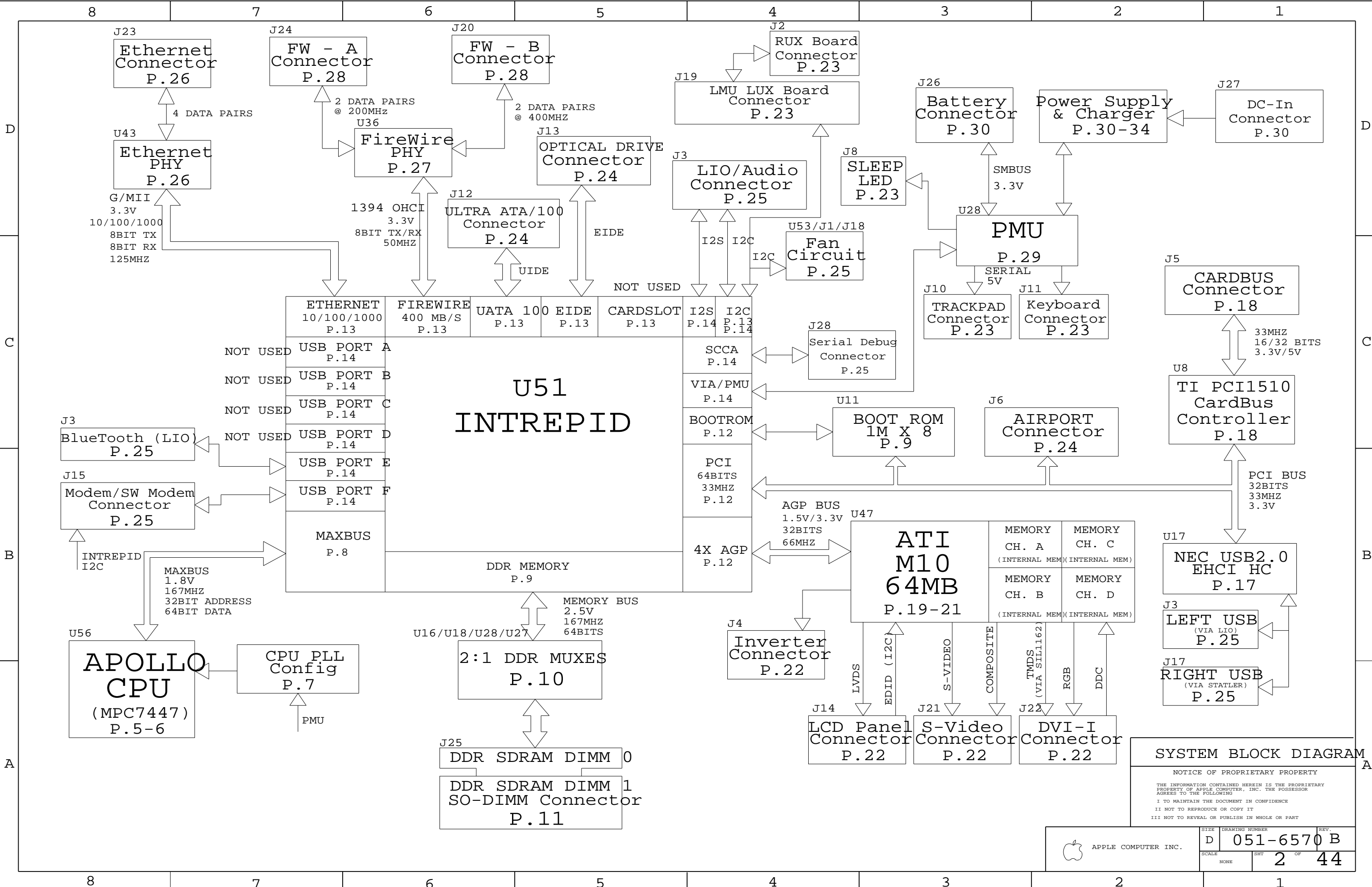


[illegible]



SYSTEM BLOCK DIAGRAM

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**POWER SYSTEM ARCHITECTURE**

The diagram illustrates the power system architecture, showing the flow of power from the AC Adapter and Backup Battery through various regulators and sequencers to the power blocks.

**Power Sources:**

- AC ADAPTER IN (PG 30)
- BACKUP BATTERY (CHARGER INPUT & BOOST OUTPUT PG 31)
- 3S 2P 18650 CELLS

**Regulators and Sequencers:**

- INRUSH LIMITER (PG 30)
- BUCK REGULATOR (LTC1625) (PG 31)
- DC/DC (LTC3707) (PG 32)
- DC/DC (LTC3411) (PG 34)
- DC/DC (MAX1715) (PG 34)
- DC/DC (MAX1717) (PG 33)
- DC/DC (MAX1772) (PG 30)
- GPU\_VCORE SEQUENCING
- MAXBUS SEQUENCING

**Power Blocks:**

- MAP31 DDR CORE
- MAP31 DDR I/O
- DDR POWER
- INTREPID CORE
- AGP I/O
- GPU\_VCORE (+1.2V)
- CPU\_VCORE (+1.385V)

**Timing Diagram:**

The timing diagram shows the sequence of power-up and shutdown events:

- SHUT-DOWN
- SLEEP
- DCDC\_EN
- DCDC\_EN\_L
- +5V\_MAIN
- +5V\_SLEEP
- +3V\_MAIN
- +3V\_SLEEP
- 3V\_5V\_OK
- +2\_5V\_MAIN
- +2\_5V\_SLEEP
- +1\_5V\_MAIN
- +1\_5V\_SLEEP
- 1\_5V\_2\_5V\_OK (MAX1715 OUTPUT)
- 1\_5V\_2\_5V\_OK (AT LTC1778 RUN/SS)
- GPU\_VCORE (D3HOT)
- GPU\_VCORE (D3COLD)

**POWER BLOCK DIAGRAM**

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D 051-6570 B

SCALE NONE SHT 3 OF 44

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**POWER BLOCK DIAGRAM**

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Apple Computer Inc. 051-6570 B 3 OF 44

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- MAP31 DDR I/O
- DDR POWER
- INTREPID CORE
- AGP I/O
- CPU\_VCORE (+1.385V)
- GPU\_VCORE (+1.2V)

**Timing Diagram:**

The timing diagram shows the sequence of power transitions during SHUT-DOWN, RUN, SLEEP, and SHUT-DOWN. Key signals include:

- SLEEP
- SLEEP\_L\_LSE
- DCDC\_EN
- DCDC\_EN\_L
- +5V\_MAIN
- +5V\_SLEEP
- +3V\_MAIN
- +3V\_SLEEP
- 3V\_5V\_OK
- +2\_5V\_MAIN
- +2\_5V\_SLEEP
- +1\_5V\_MAIN
- +1\_5V\_SLEEP
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- GPU\_VCORE (D3HOT)
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**Power Block Diagram**

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D 051-6570 B

SCALE NONE SHT 3 OF 44

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN  
1/2 OZ CU THICKNESS: 0.7 MILS  
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%  
DIELECTRIC: FR-4  
LAYER COUNT: 10  
SIGNAL TRACE WIDTH: 4 MILS  
SIGNAL TRACE SPACING: 4 MILS  
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

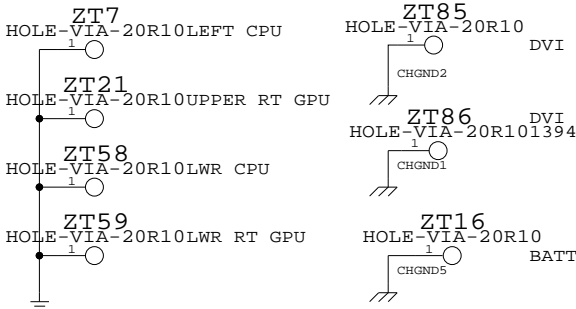
BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA				SIGNAL (1/2 OZ + COPPER PLATING)			
1				SIGNAL (1/2 OZ + COPPER PLATING)			
2	PREPREG (3 MIL)			SIGNAL (1/2 OZ)			
3	PREPREG (3 MIL)			GROUND (1/2 OZ)			
4	CORE (3 MIL)			SIGNAL (1/2 OZ)			
5	PREPREG (5 MIL)			CUT POWER PLANE (1 OZ)			
6	CORE (5 MIL)			CUT POWER PLANE (1 OZ)			
7	PREPREG (5 MIL)			SIGNAL (1/2 OZ)			
8	CORE (3 MIL)			GROUND (1/2 OZ)			
9	PREPREG (3 MIL)			SIGNAL (1/2 OZ)			
10	PREPREG (3 MIL)			SIGNAL (1/2 OZ + COPPER PLATING)			

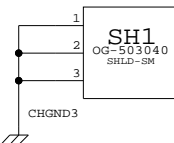
BOARD HOLES

CHASSIS MOUNTS

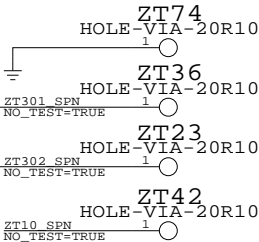
ASICS HEATSINK MOUNTS I/O AREA



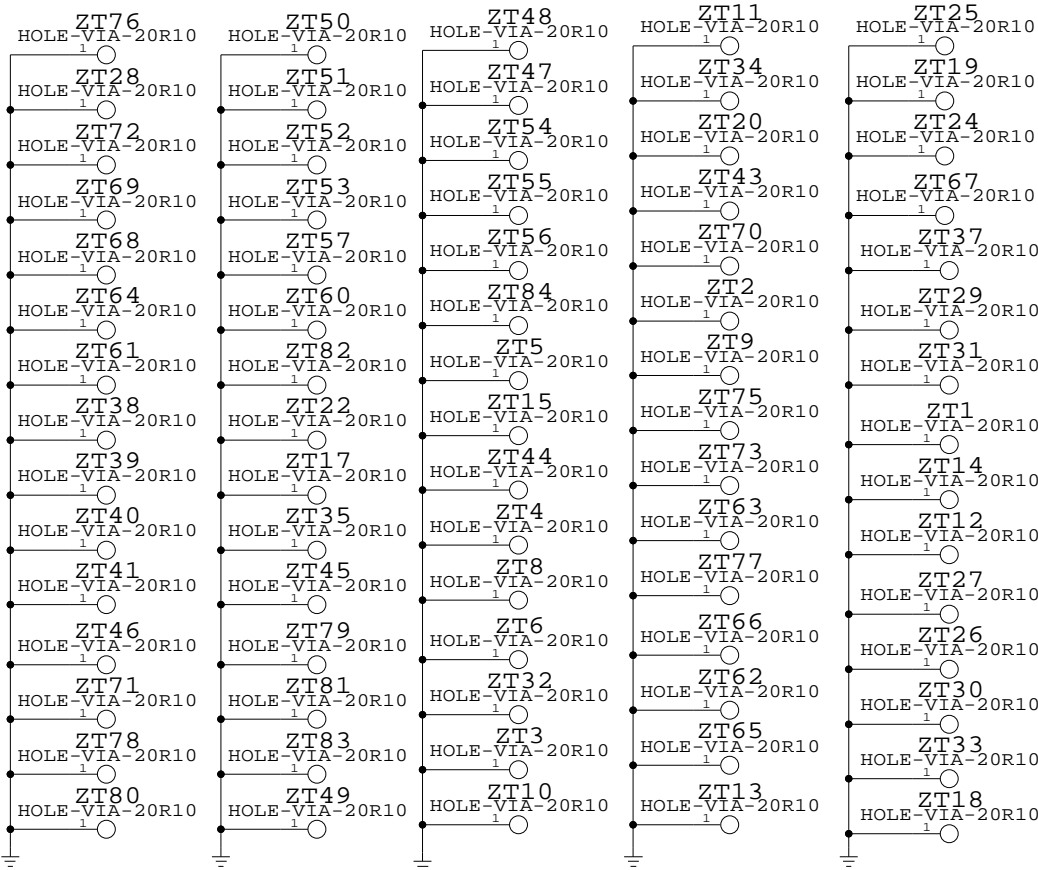
INVERTER



MECH. HOLES



GROUND VIAS



BOARD INFORMATION

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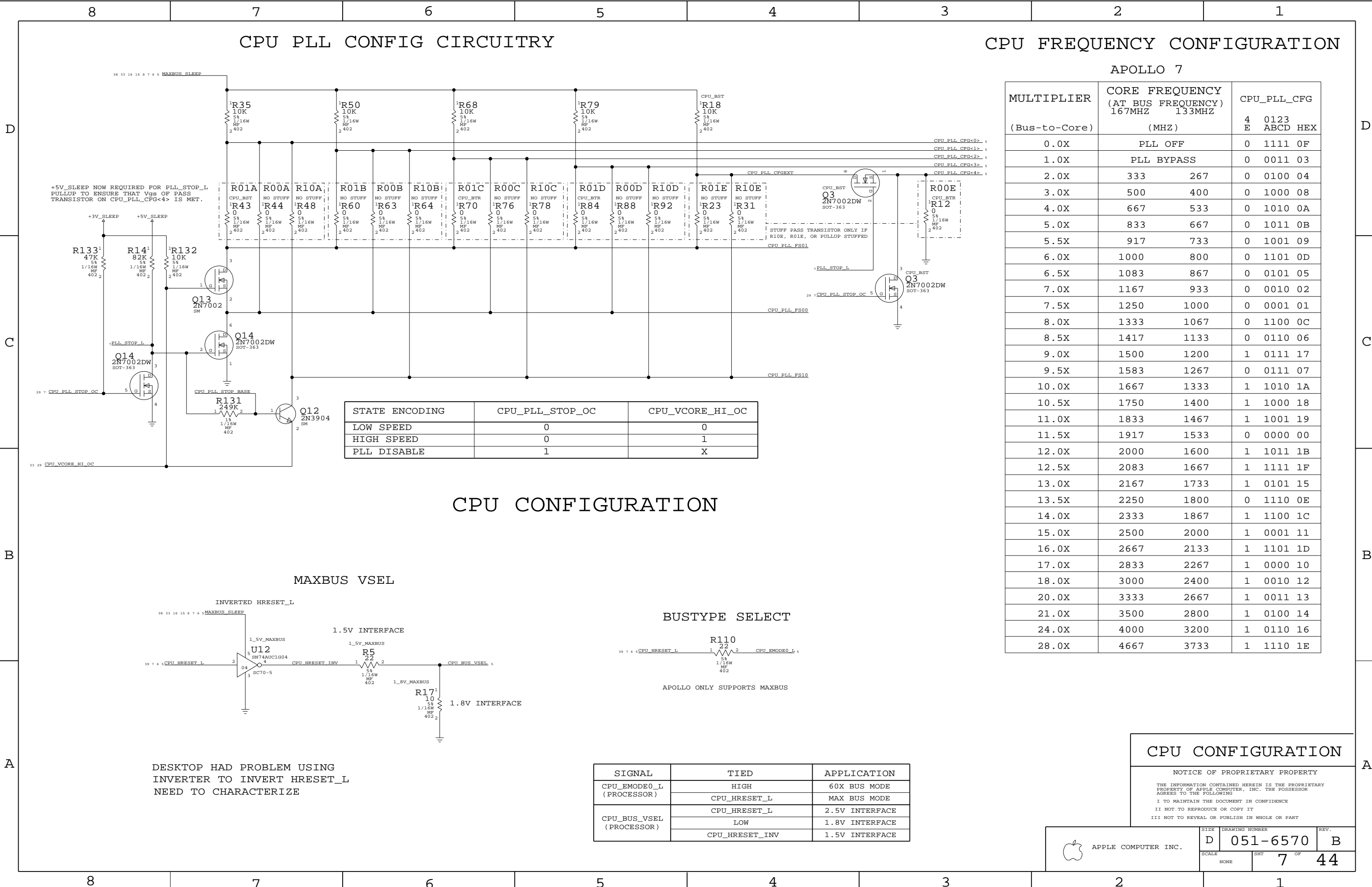


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SIZE	D	DRAWING NUMBER	051-6570	REV.	B
SCALE	NONE	SHT	4	OF	44

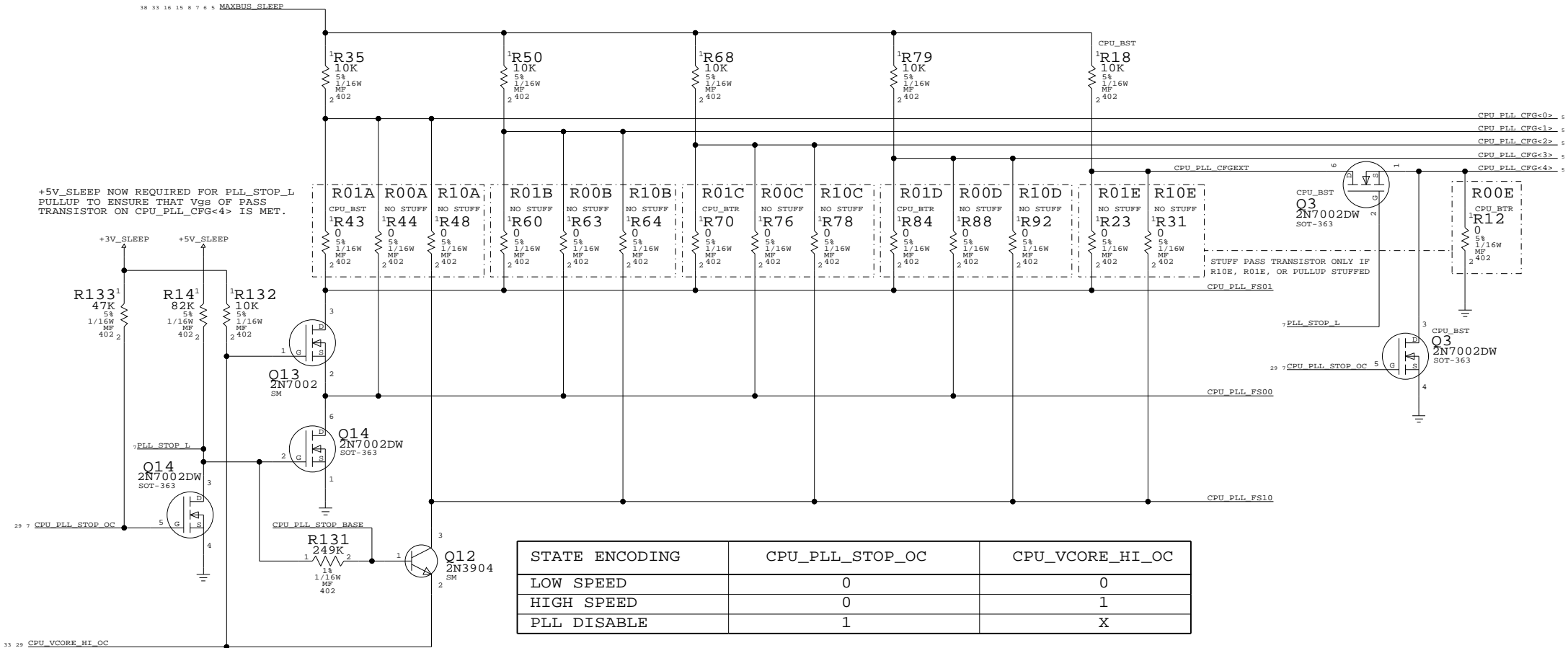






CPU PLL CONFIG CIRCUITRY

CPU FREQUENCY CONFIGURATION

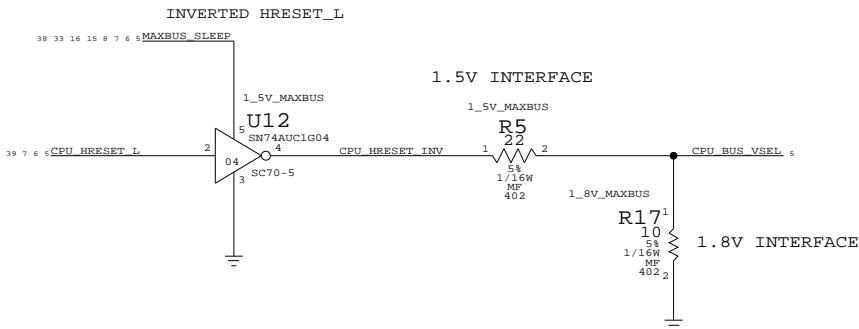


STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY)		CPU_PLL_CFG		
	167MHZ	133MHZ	4 E	0123 ABCD	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

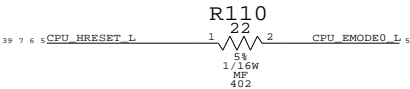
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING  
INVERTER TO INVERT HRESET\_L  
NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

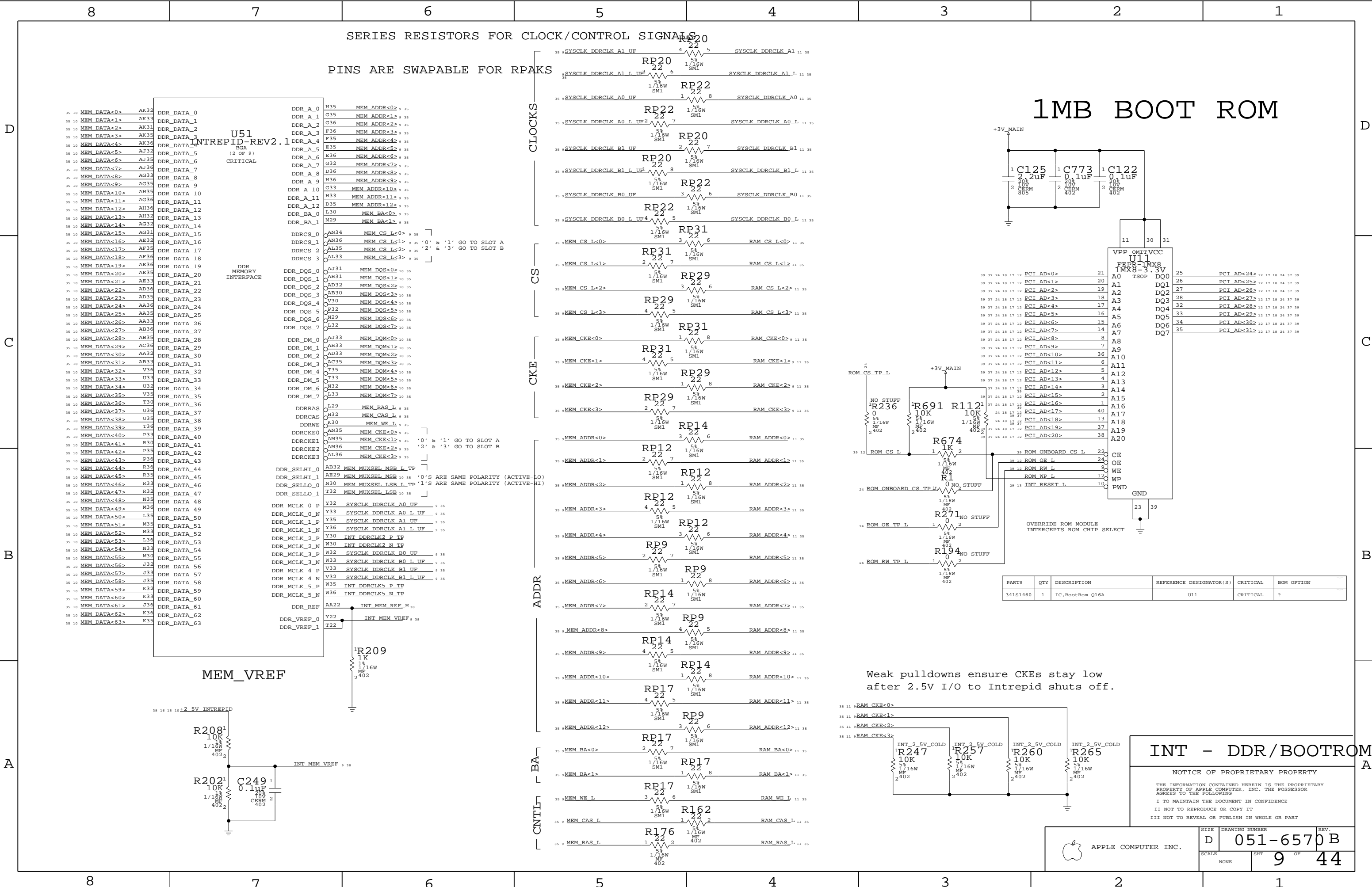
CPU CONFIGURATION

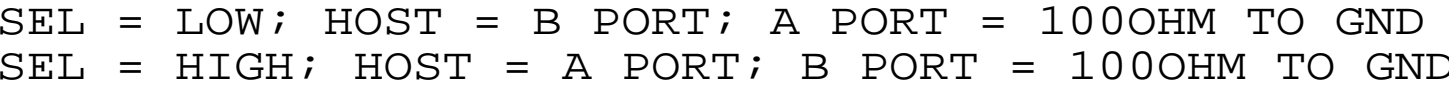
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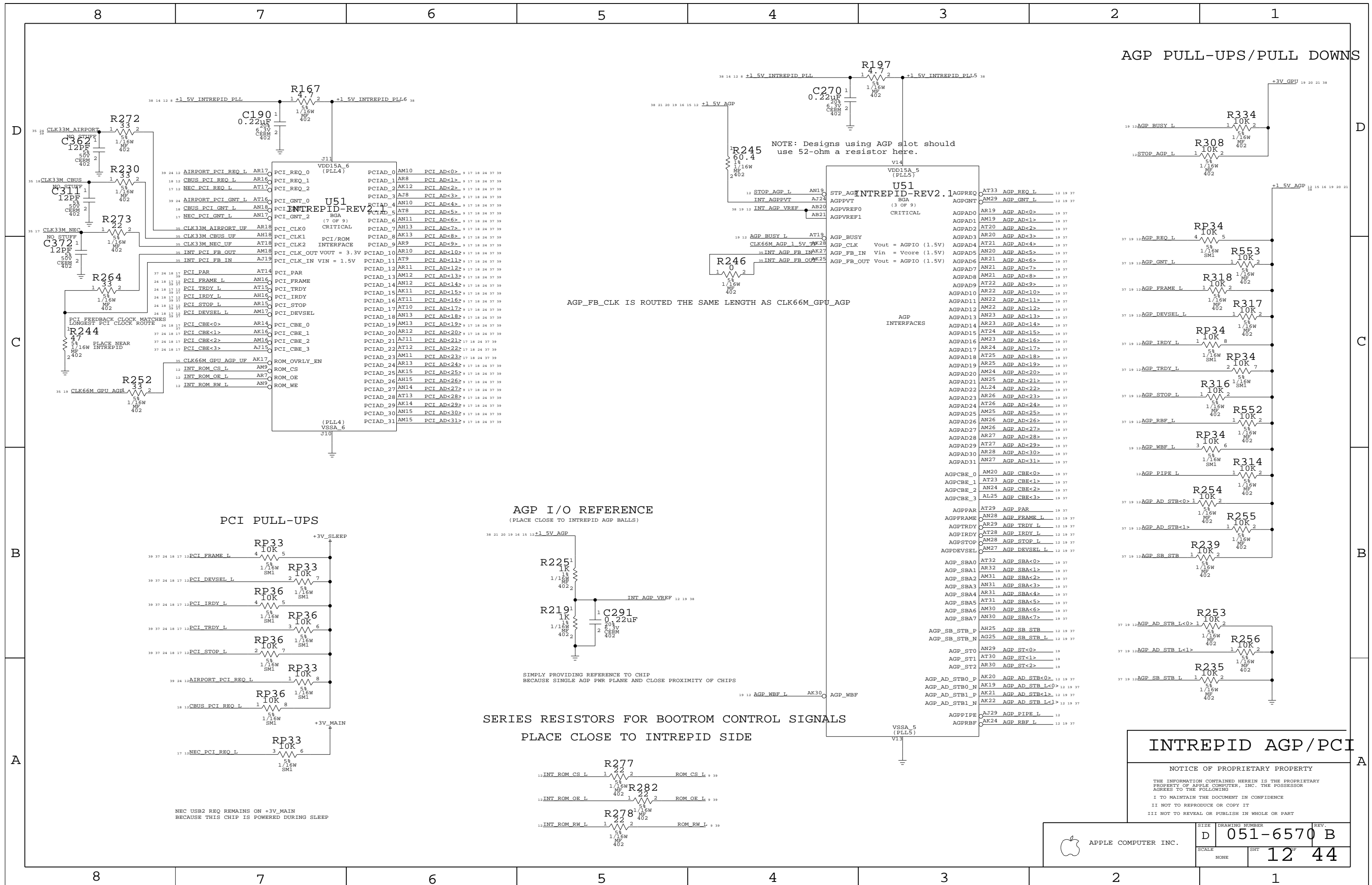
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER		REV.
	D	051-6570	B	
SCALE		SHT	7 OF	44
NONE				





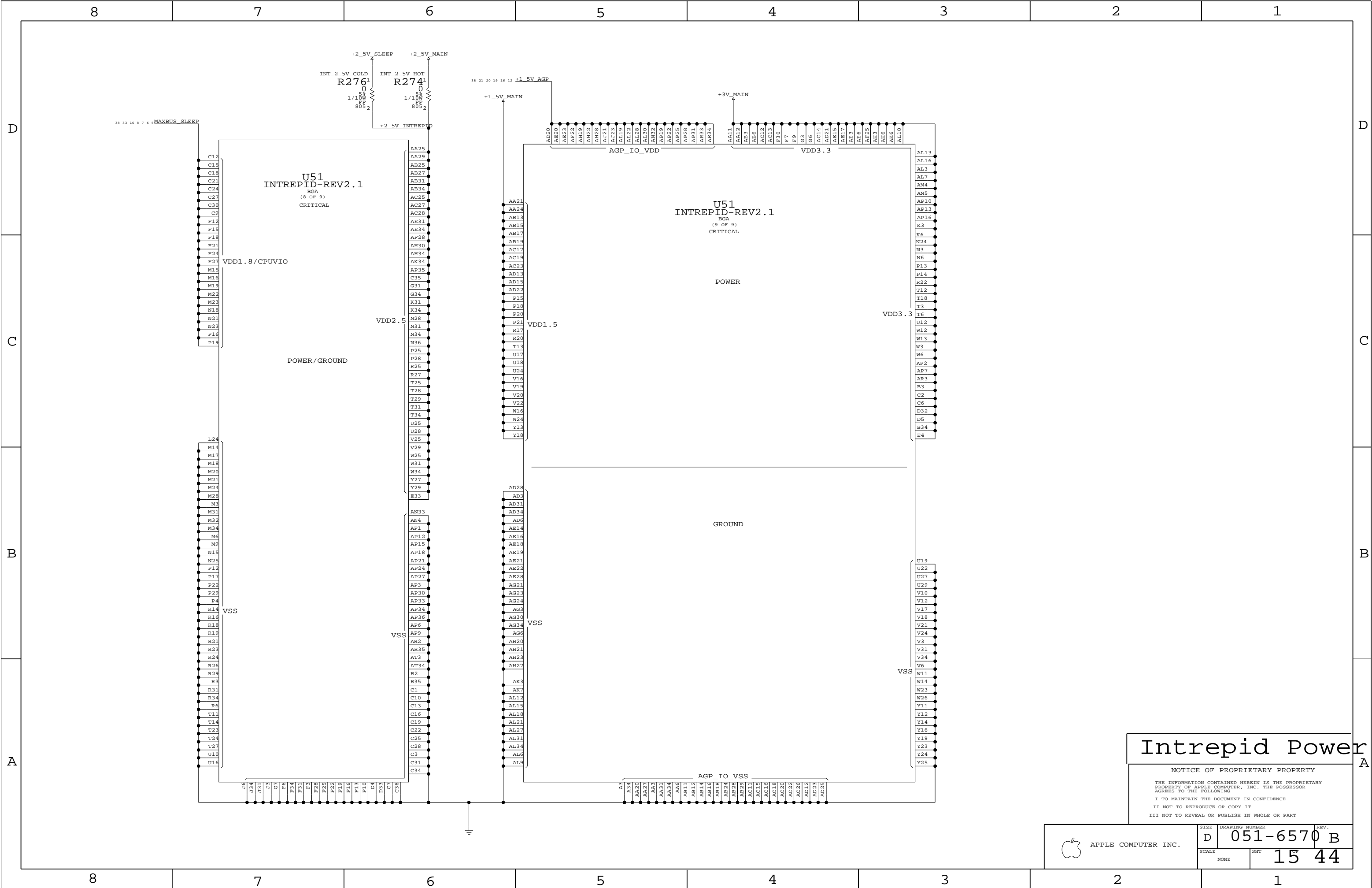












# Intrepid Power

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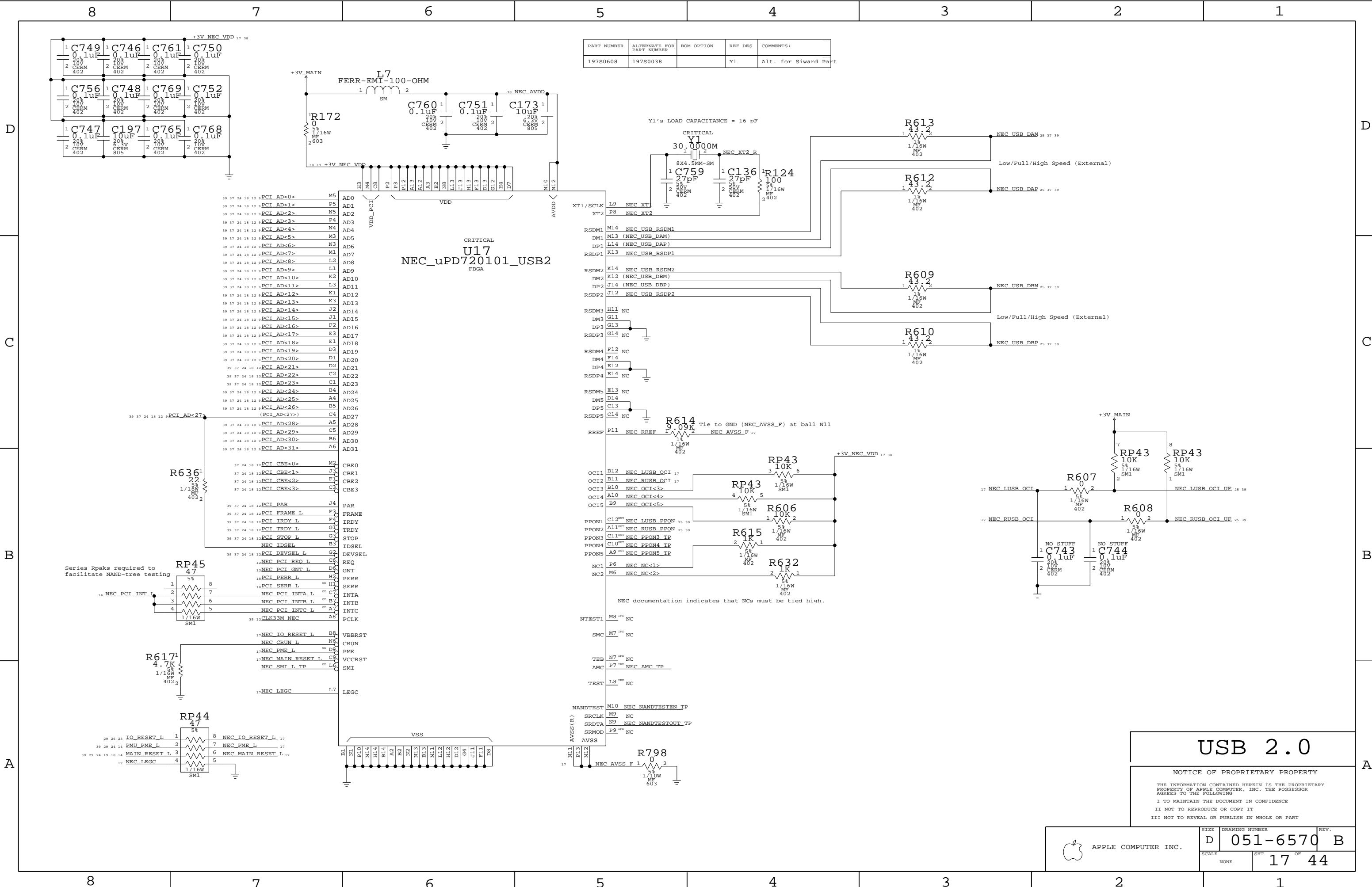
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D	051-6570	B
SCALE	SHT	
NONE	15	44





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
197S0608	197S0038		Y1	Alt. for Siward Part

USB 2.0

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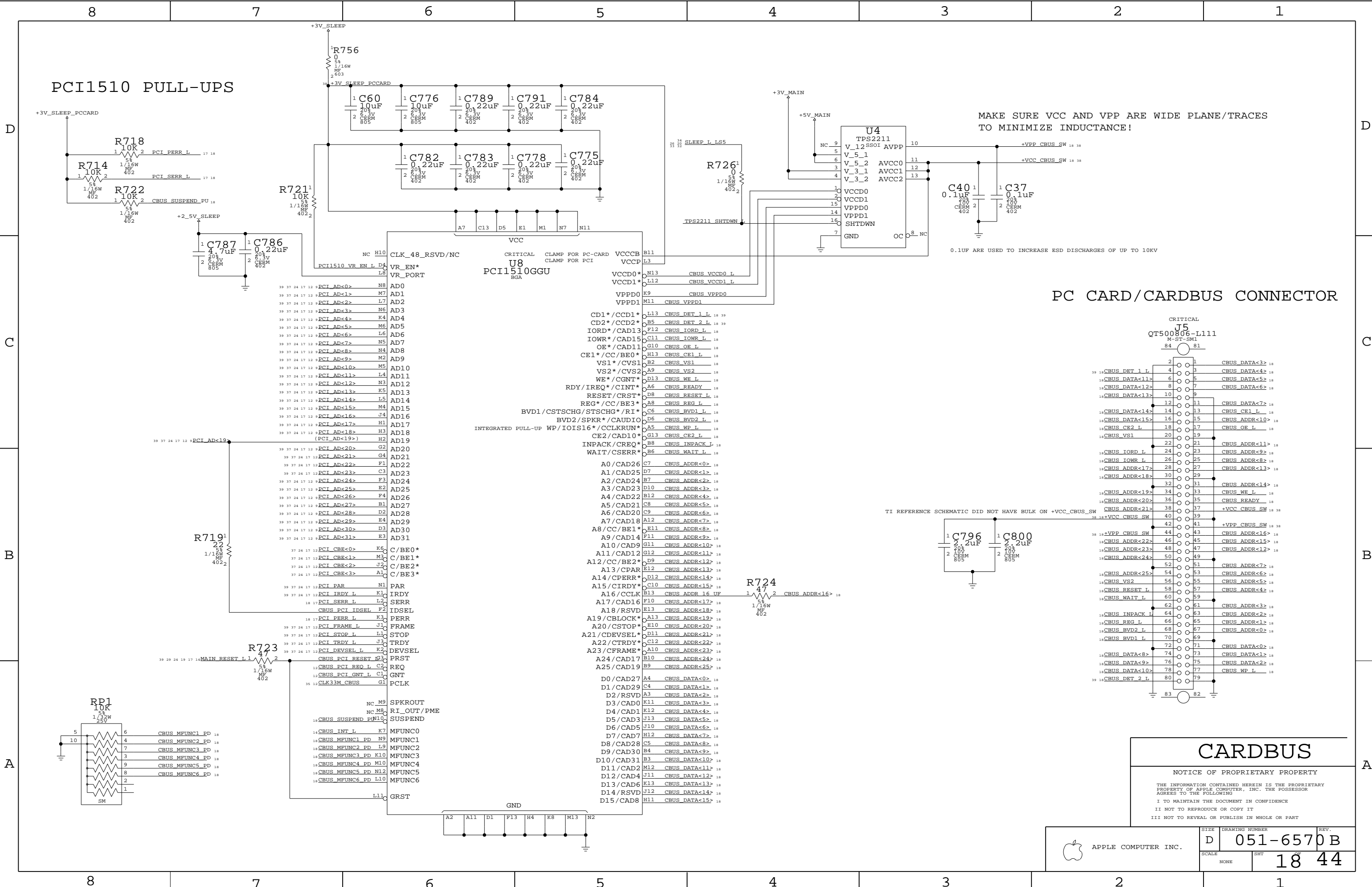
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	D	051-6570	B
SCALE	SHT		OF
	NONE		17 44



MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

PC CARD/CARDBUS CONNECTOR

CARDBUS

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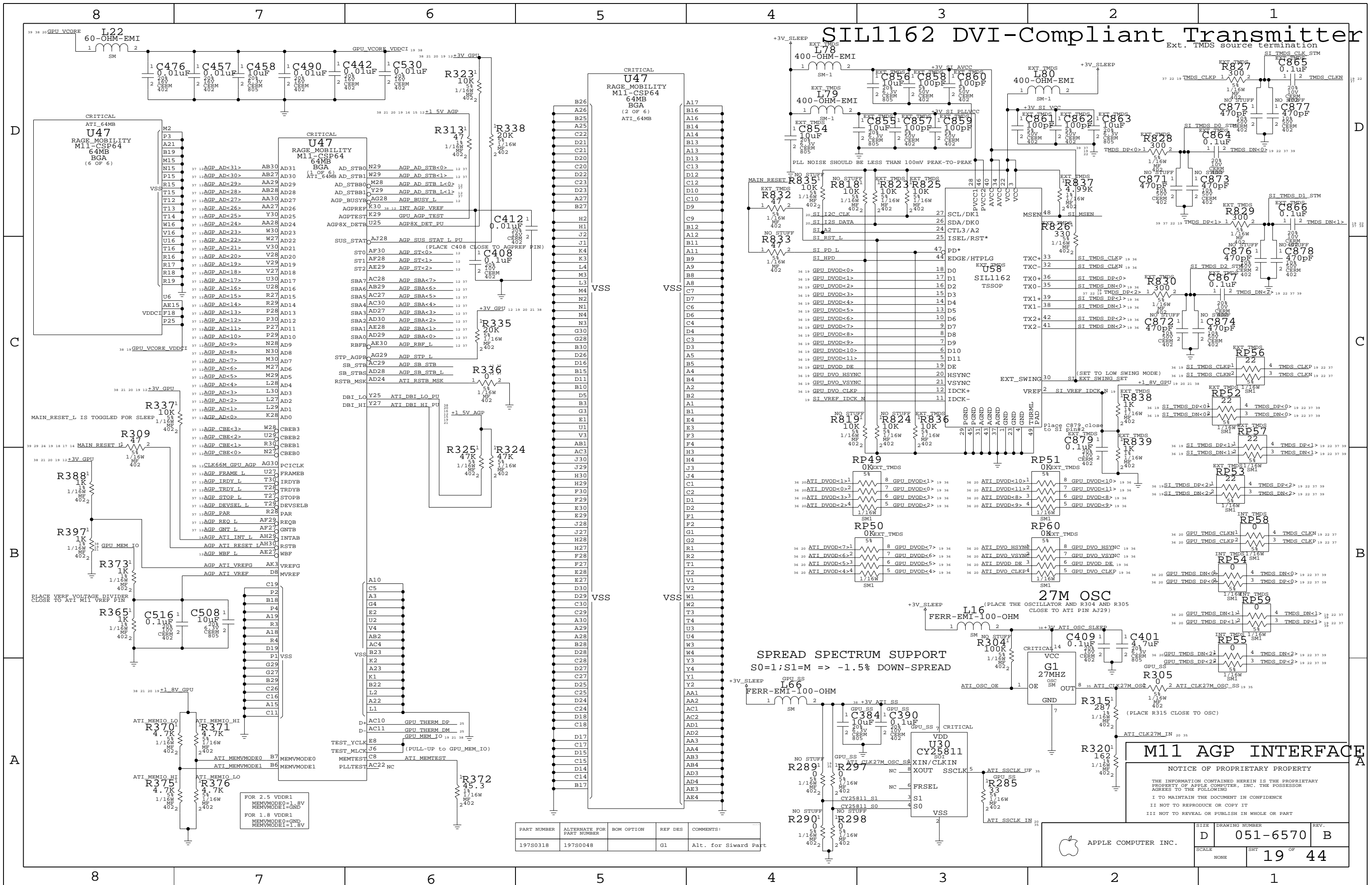
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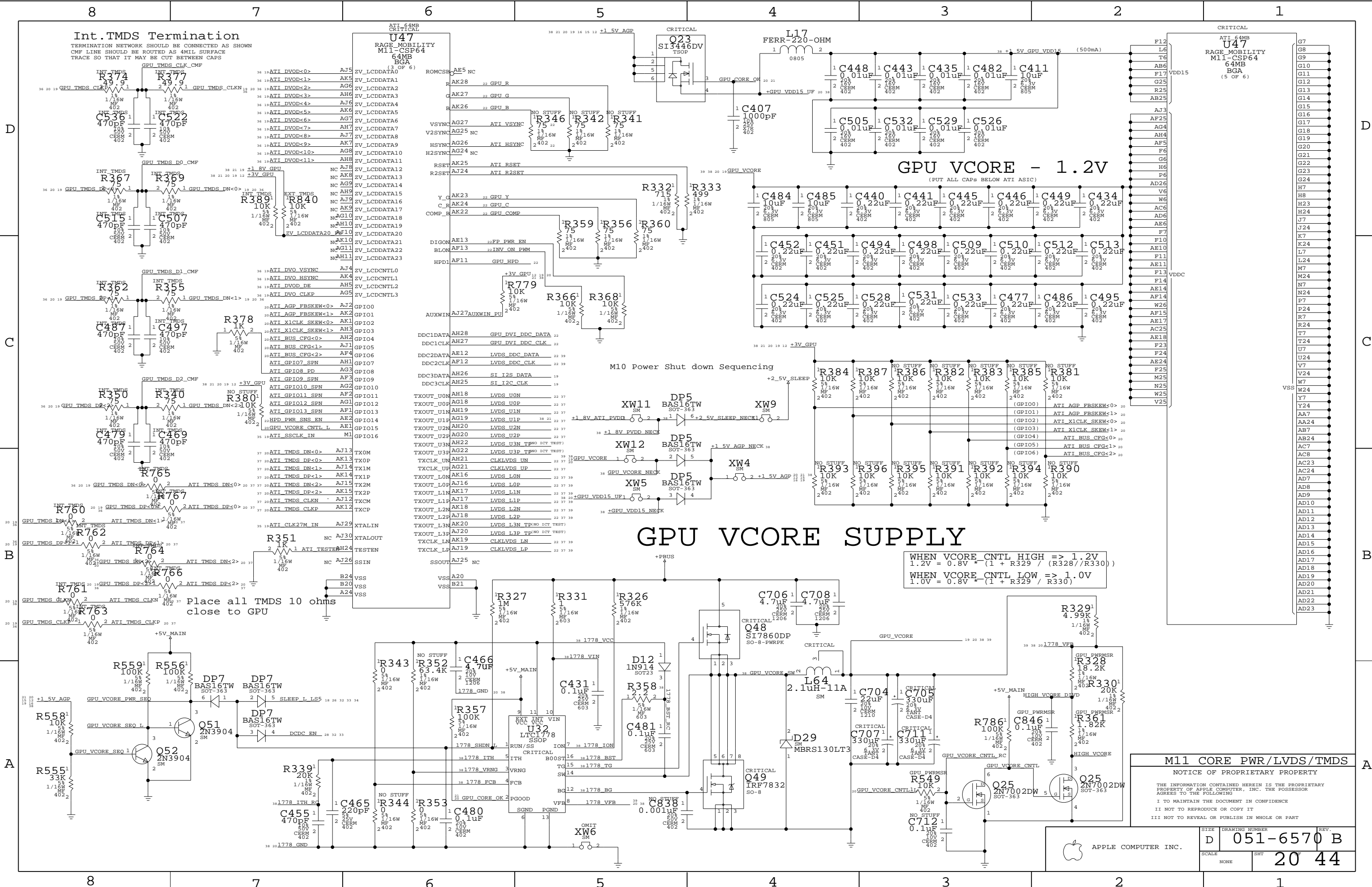
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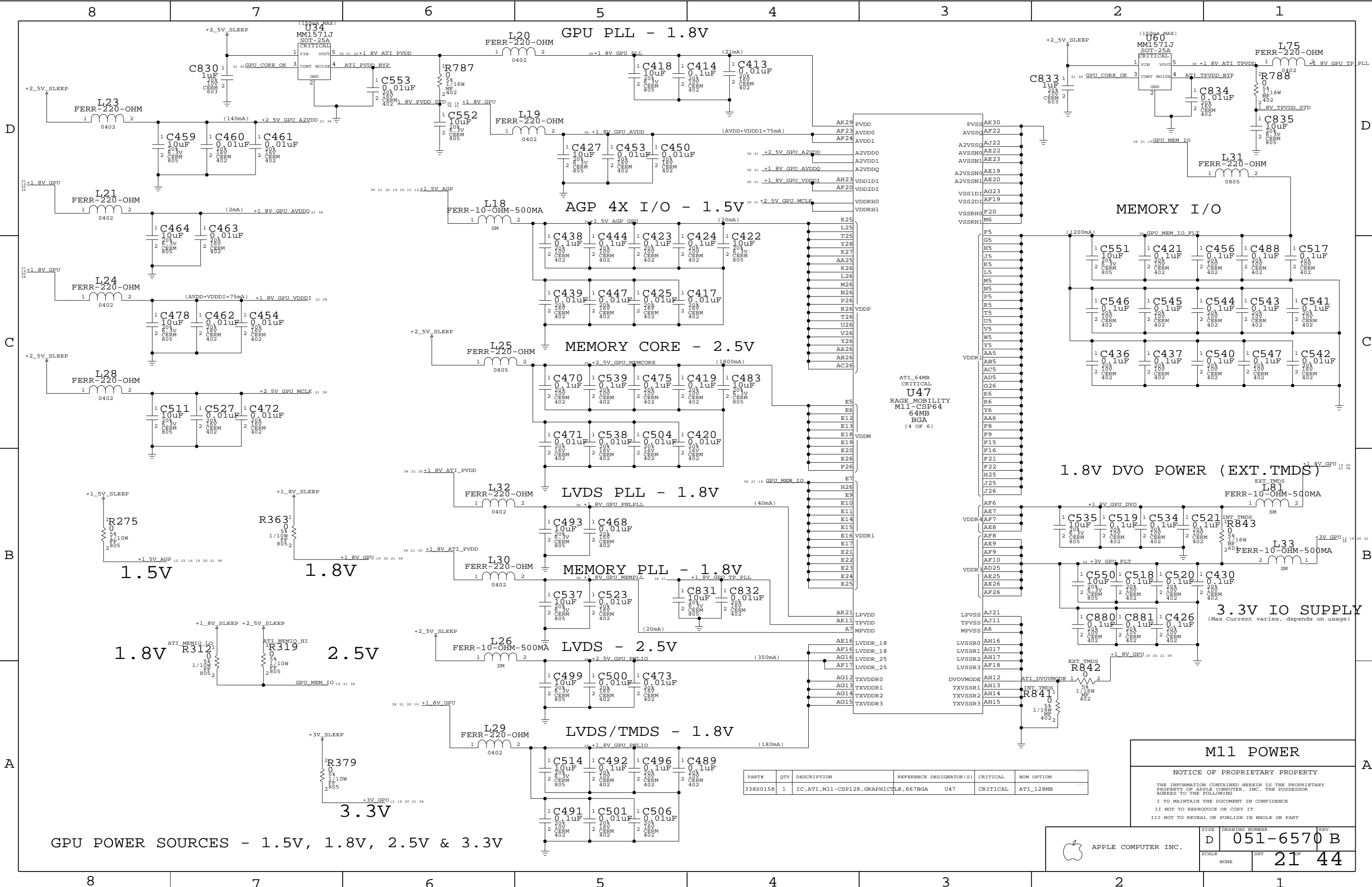
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6570 B	
SCALE	NONE	SHT	18 44





Int.TMDS Termination  
TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN  
CMP LINE SHOULD BE ROUTED AS 4MIL SURFACE  
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

M11 CORE PWR/LVDS/TMDS  
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GRAPHIC,TLR,667BGA	U47	CRITICAL	ATI_128MB

M11 POWER

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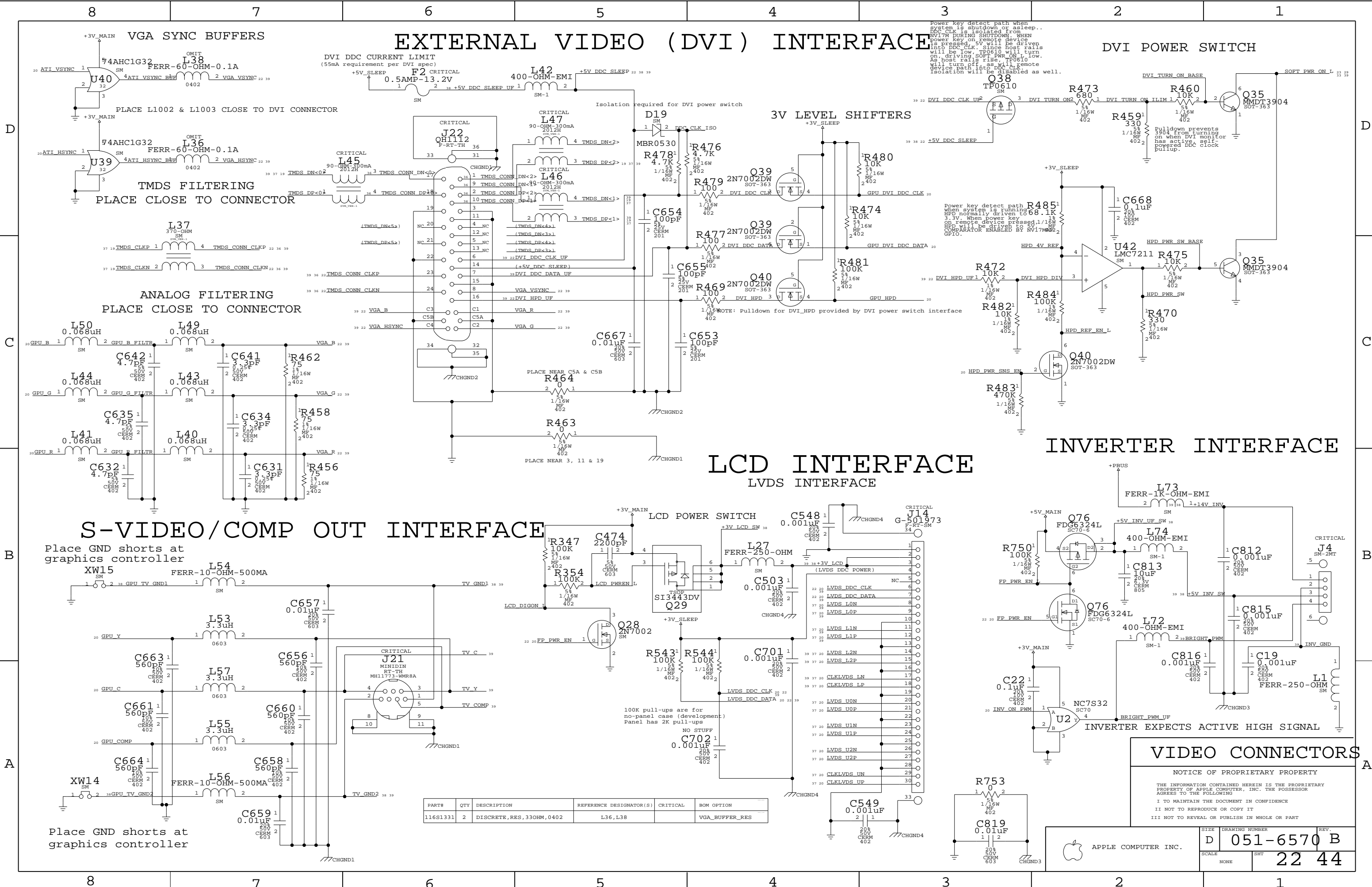
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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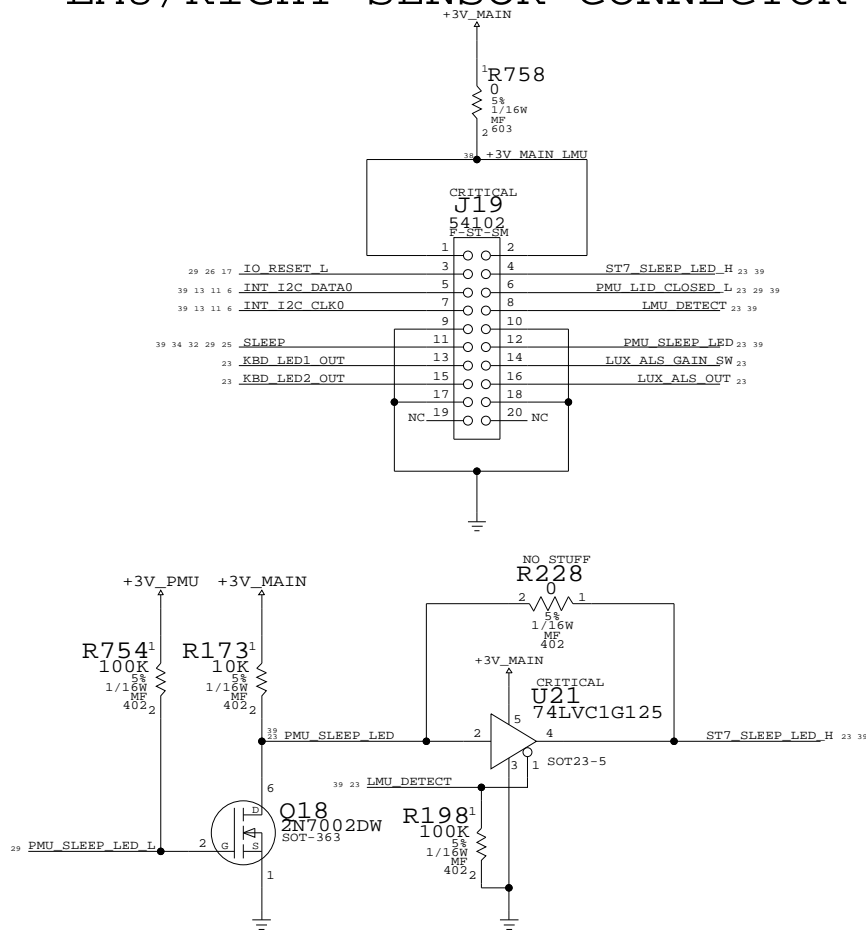
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SIZE	DRAWING NUMBER	REV.
D	051-6570 B	
SCALE	SHT	
NONE	21	44

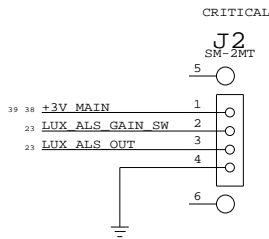
# EXTERNAL VIDEO (DVI) INTERFACE



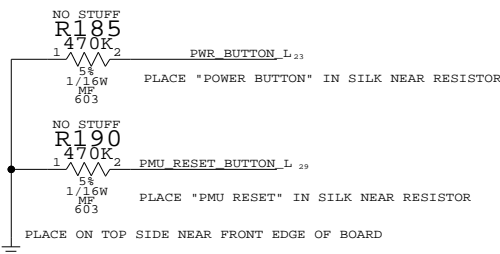
LMU/RIGHT SENSOR CONNECTOR



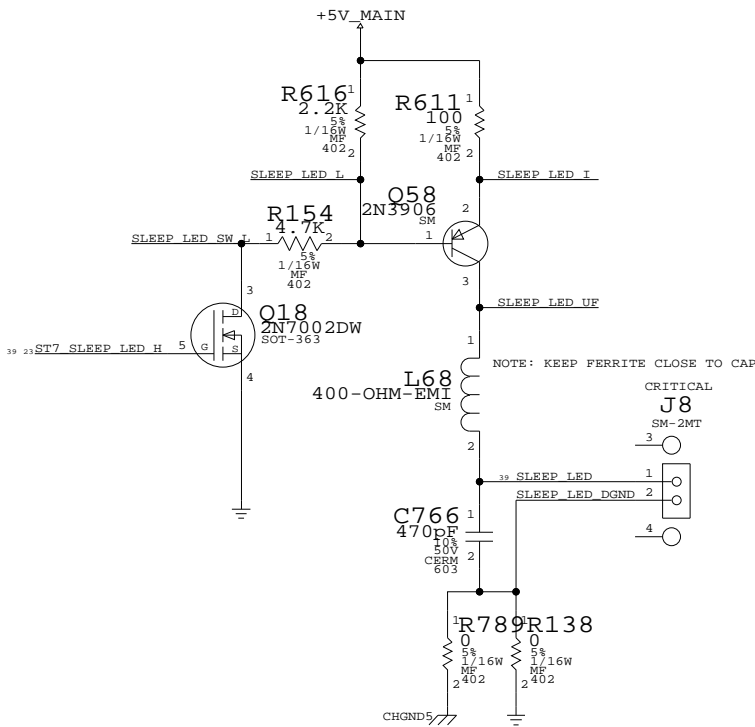
LEFT LIGHT SENSOR CONNECTOR



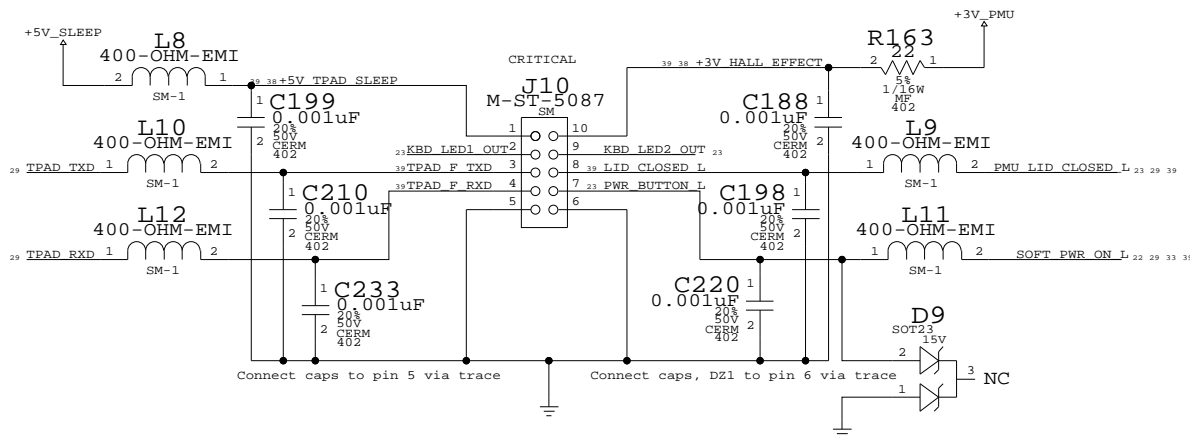
DEBUG HELPERS



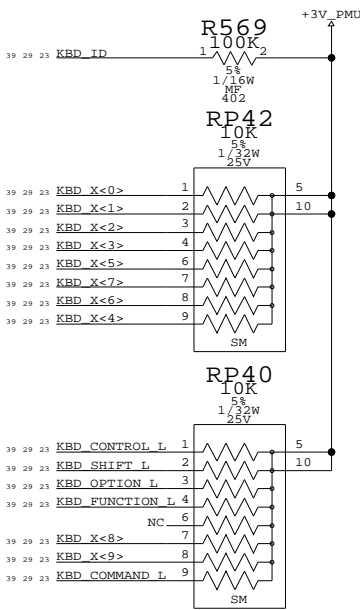
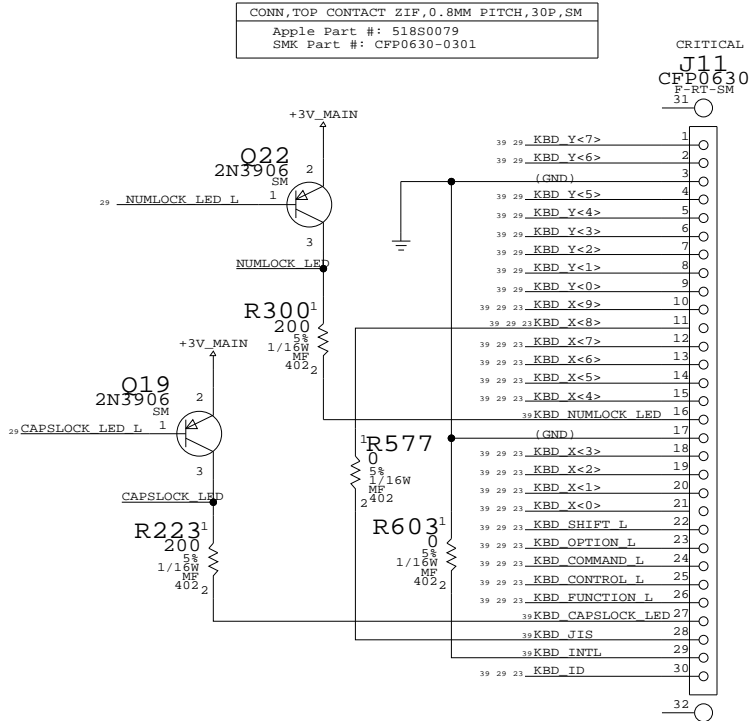
SLEEP LED



TRACKPAD/PWR BTN CONN



TOP CONTACT ZIF KEYBOARD CONN



KEYBOARD PULLUPS

KEYBOARD/TPAD/SLEEP LED

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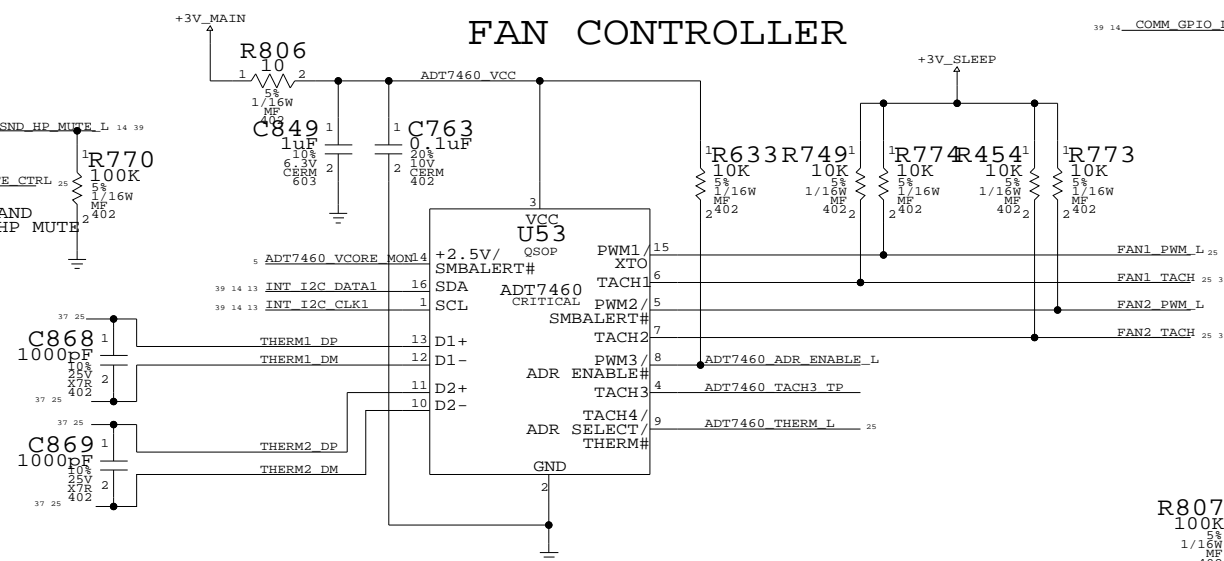
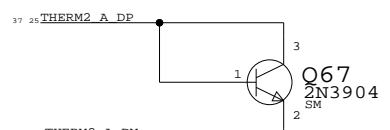
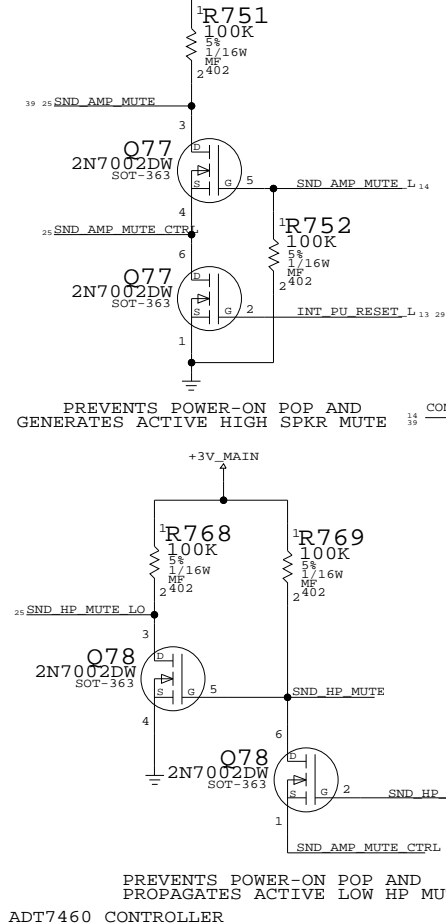


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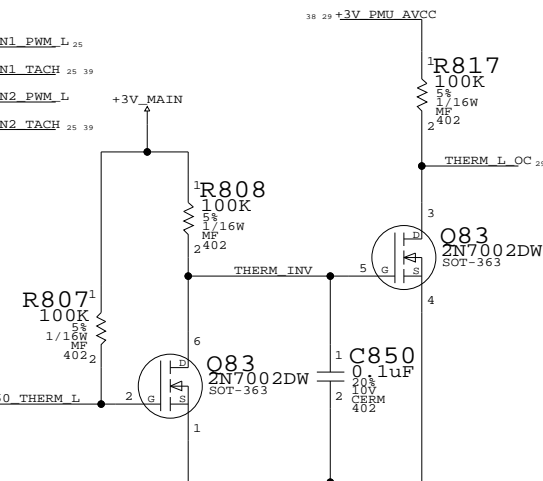
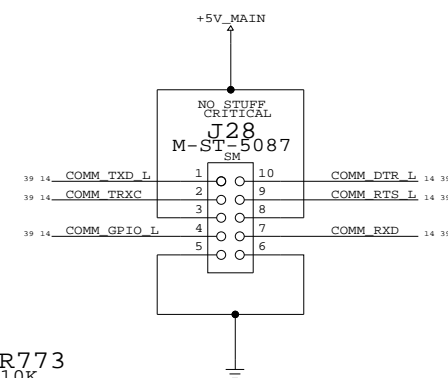
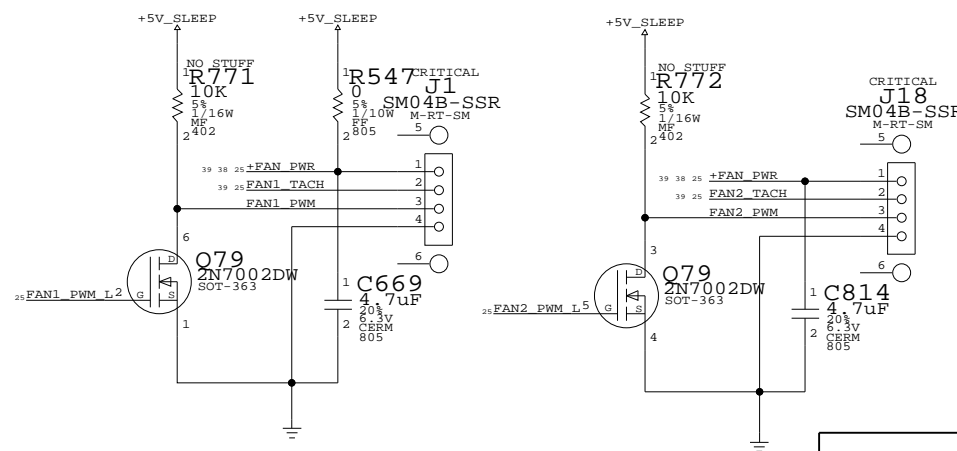
SIZE	DRAWING NUMBER	REV.
D	051-6570 B	
SCALE	SHT	OF
NONE	23	44



USB MODEM/SOFT MODEM RIGHT USB BOARD



## GPU FAN

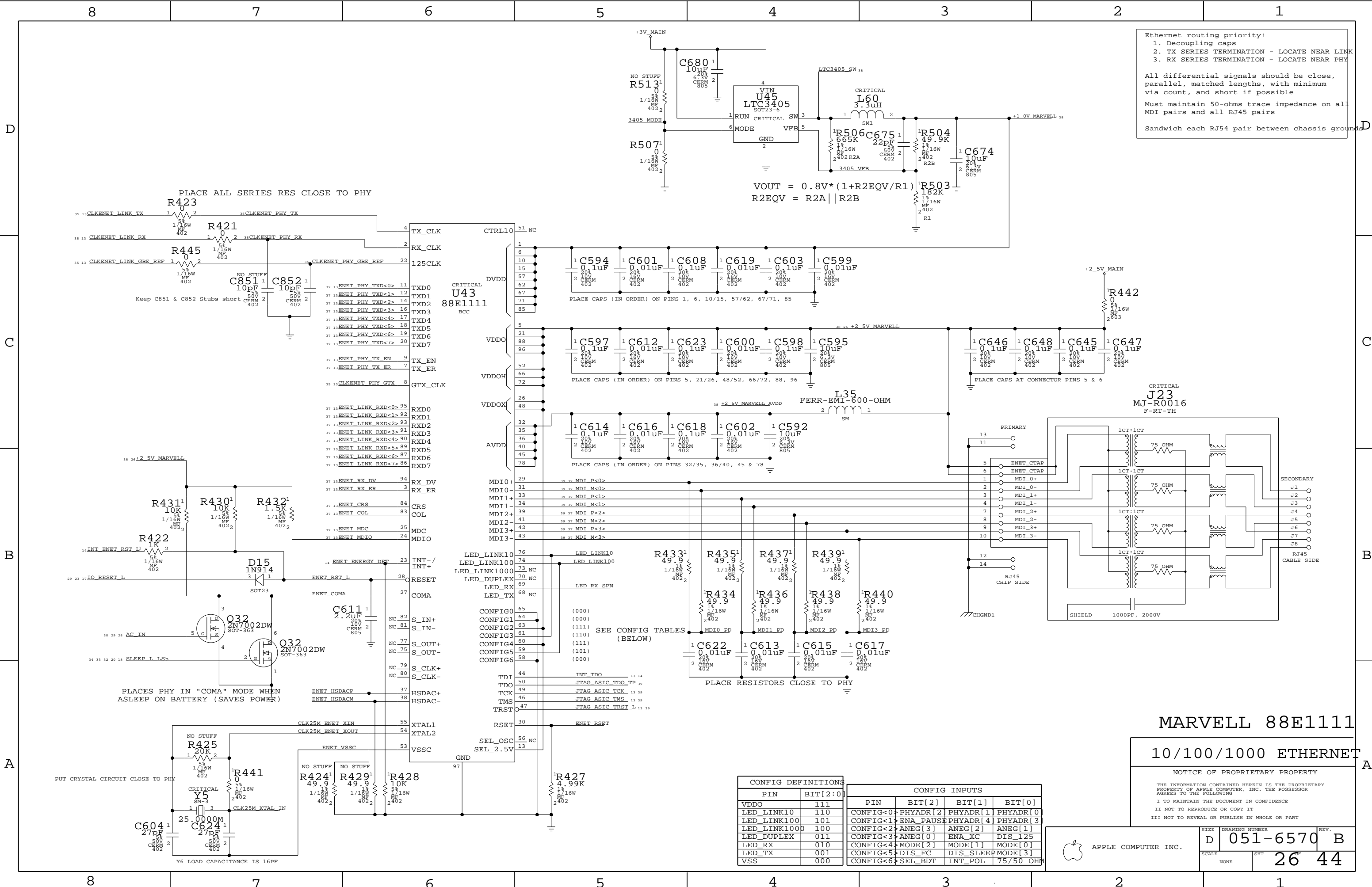


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SCALE	SHT	25 OF 4
-------	-----	---------

25 OF 4



Ethernet routing priority:  
1. Decoupling caps  
2. TX SERIES TERMINATION - LOCATE NEAR LINK  
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

MARVELL 88E1111

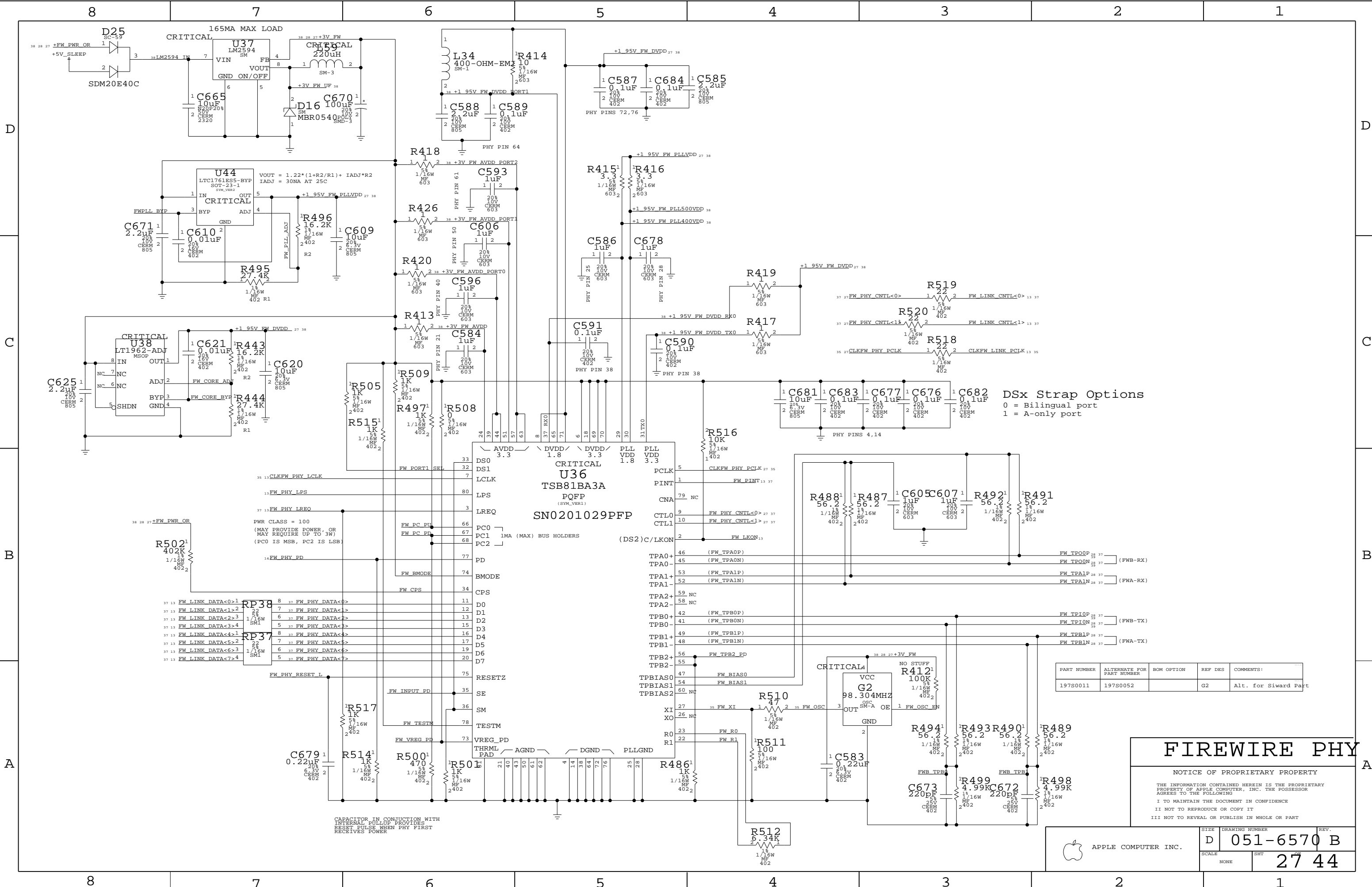
10/100/1000 ETHERNET

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	D	051-6570	B
SCALE	SHT		26 44
	NONE		

CONFIG DEFINITIONS		CONFIG INPUTS			
PIN	BIT[2:0]	PIN	BIT[2]	BIT[1]	BIT[0]
VDDO	111	CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
LED_LINK10	110	CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
LED_LINK100	101	CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
LED_LINK1000	100	CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
LED_DUPLEX	011	CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
LED_RX	010	CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
LED_TX	001	CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM
VSS	000				



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052		G2	Alt. for Siward Part

**FIREWIRE PHY**

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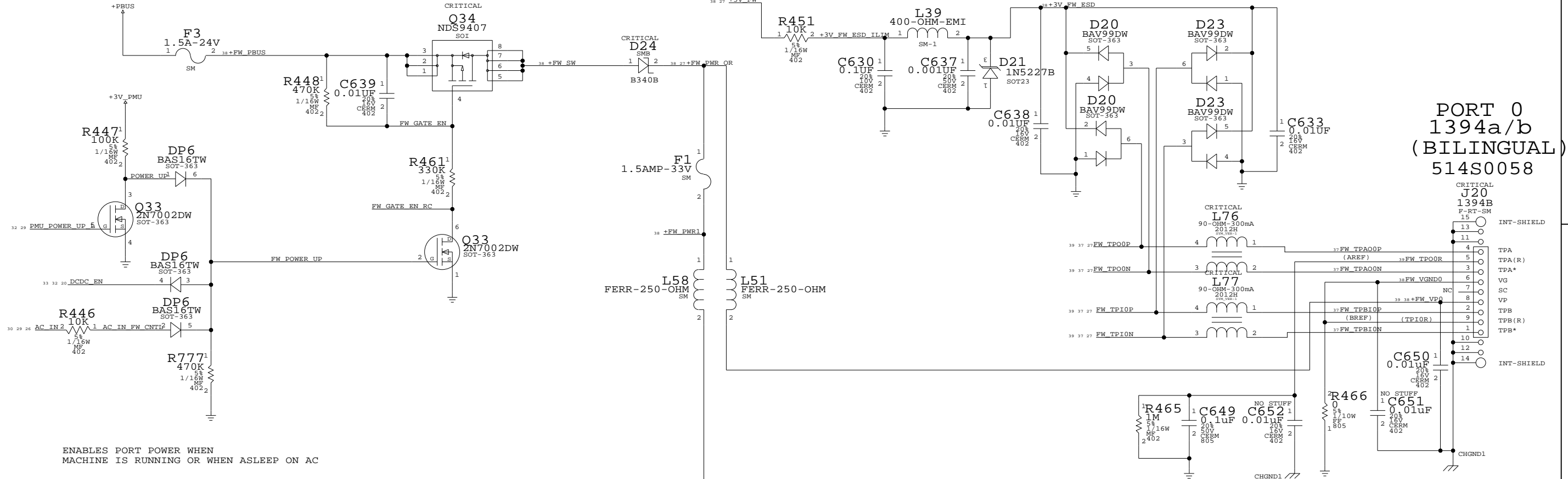
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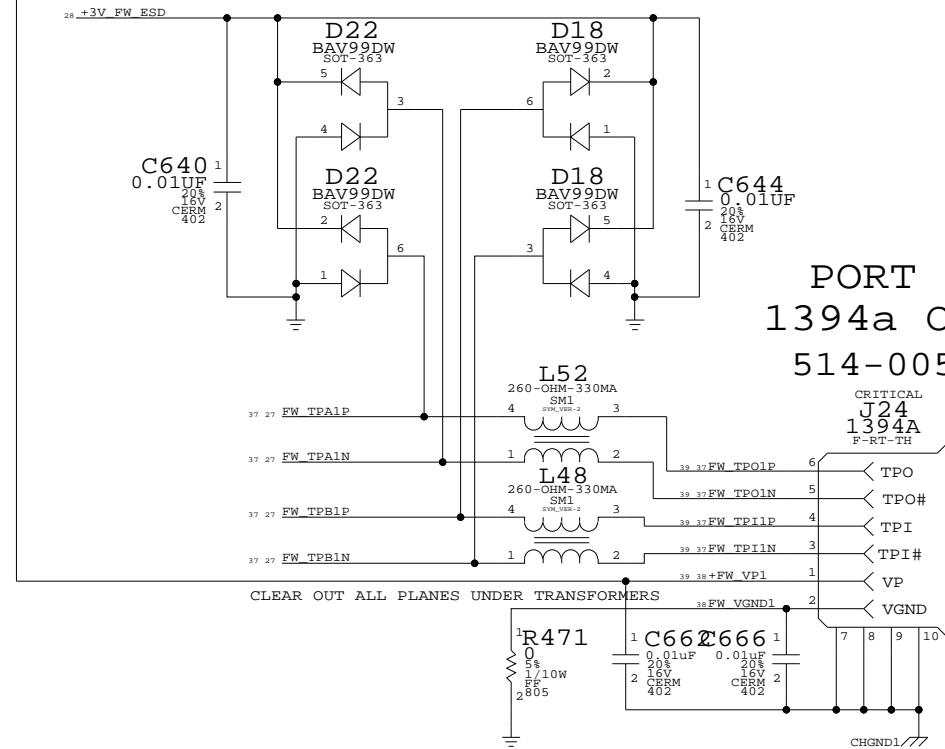
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	SCALE	SHT	
	NONE	27	44



PORT 1  
1394a ONLY  
514-0057



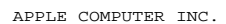
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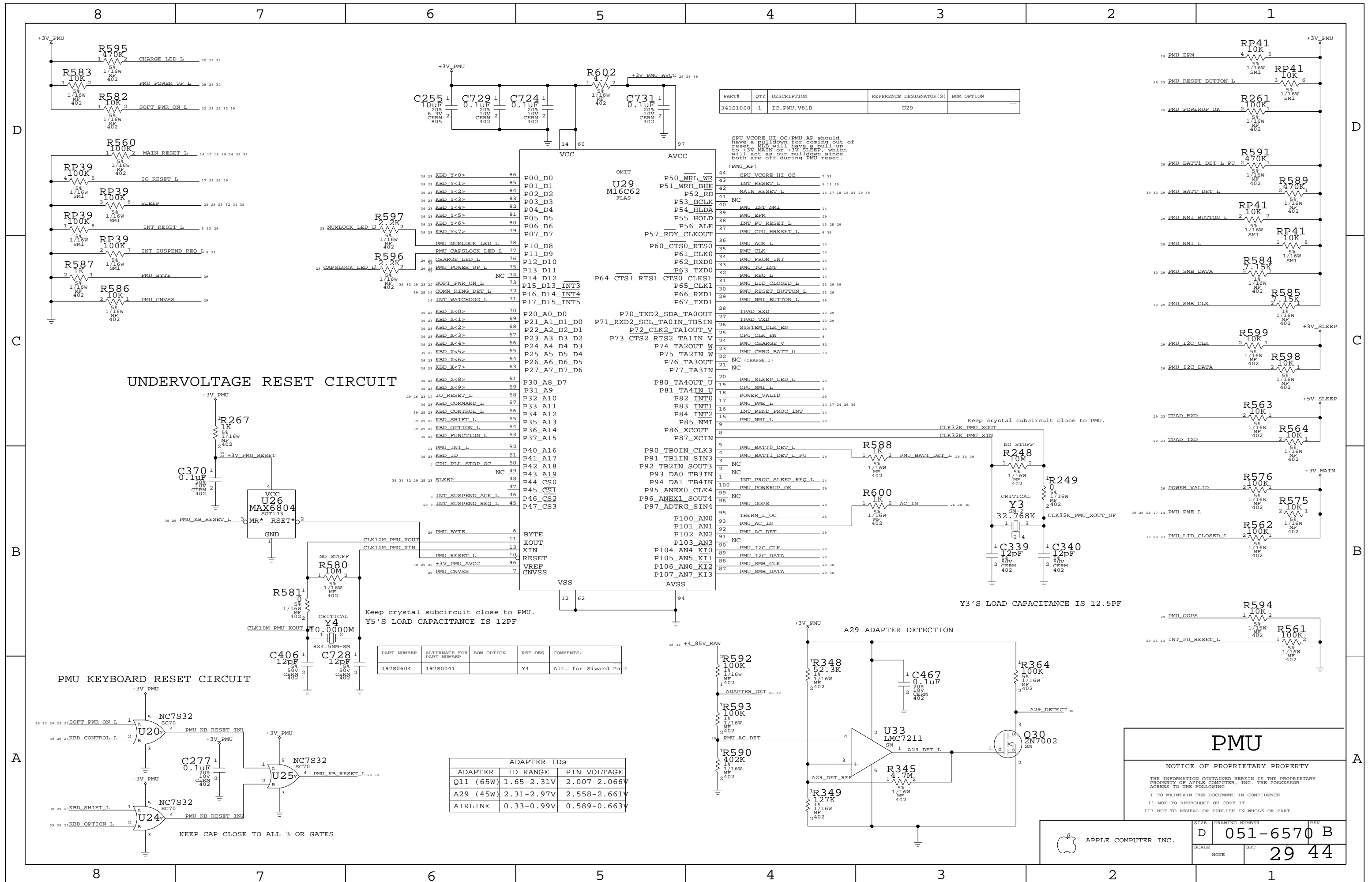
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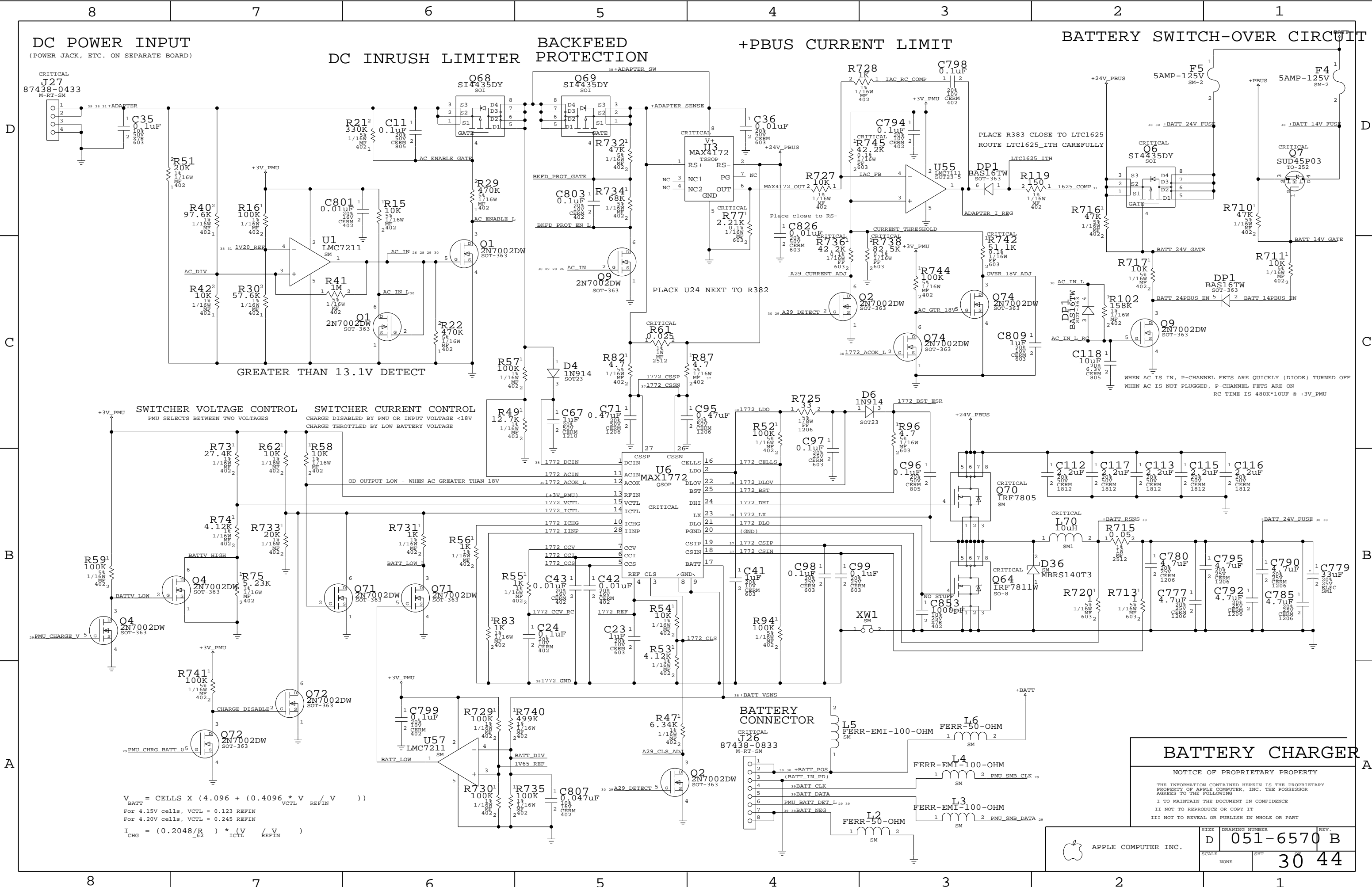


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D	051-6570 B
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SCALE	SHT	OF	
NONE	28	44	

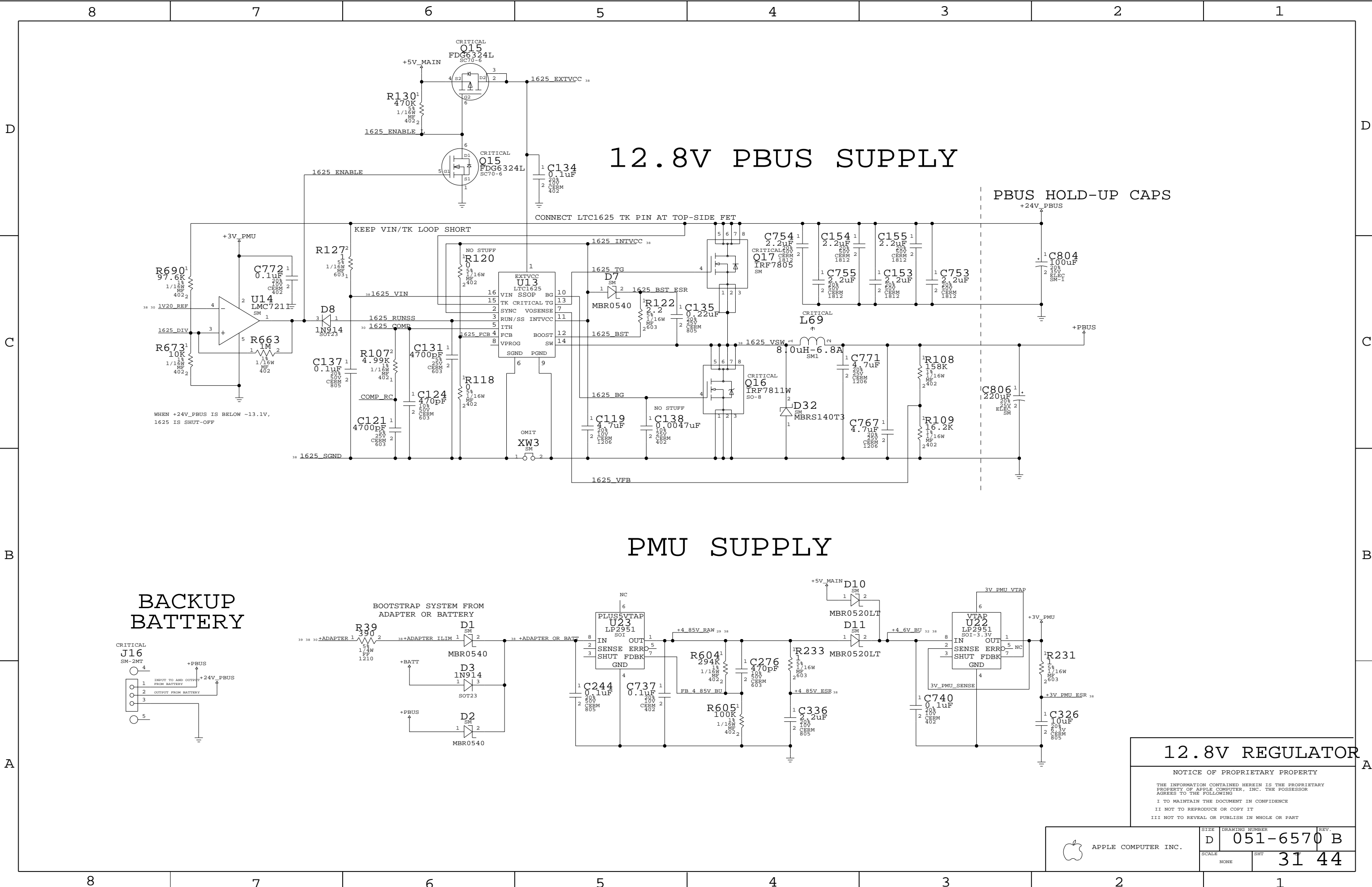




$$V_{BATT} = CELLS \times (4.096 + (0.4096 \times V_{VCTL} / V_{REFIN}))$$

For 4.15V cells,  $V_{CTL} = 0.123 \times V_{REFIN}$   
For 4.20V cells,  $V_{CTL} = 0.245 \times V_{REFIN}$

$$I_{CHG} = (0.2048 / R_{G2}) \times (V_{G2} / V_{REFIN})$$



# 12.8V PBus SUPPLY

PBUS HOLD-UP CAPS

# PMU SUPPLY

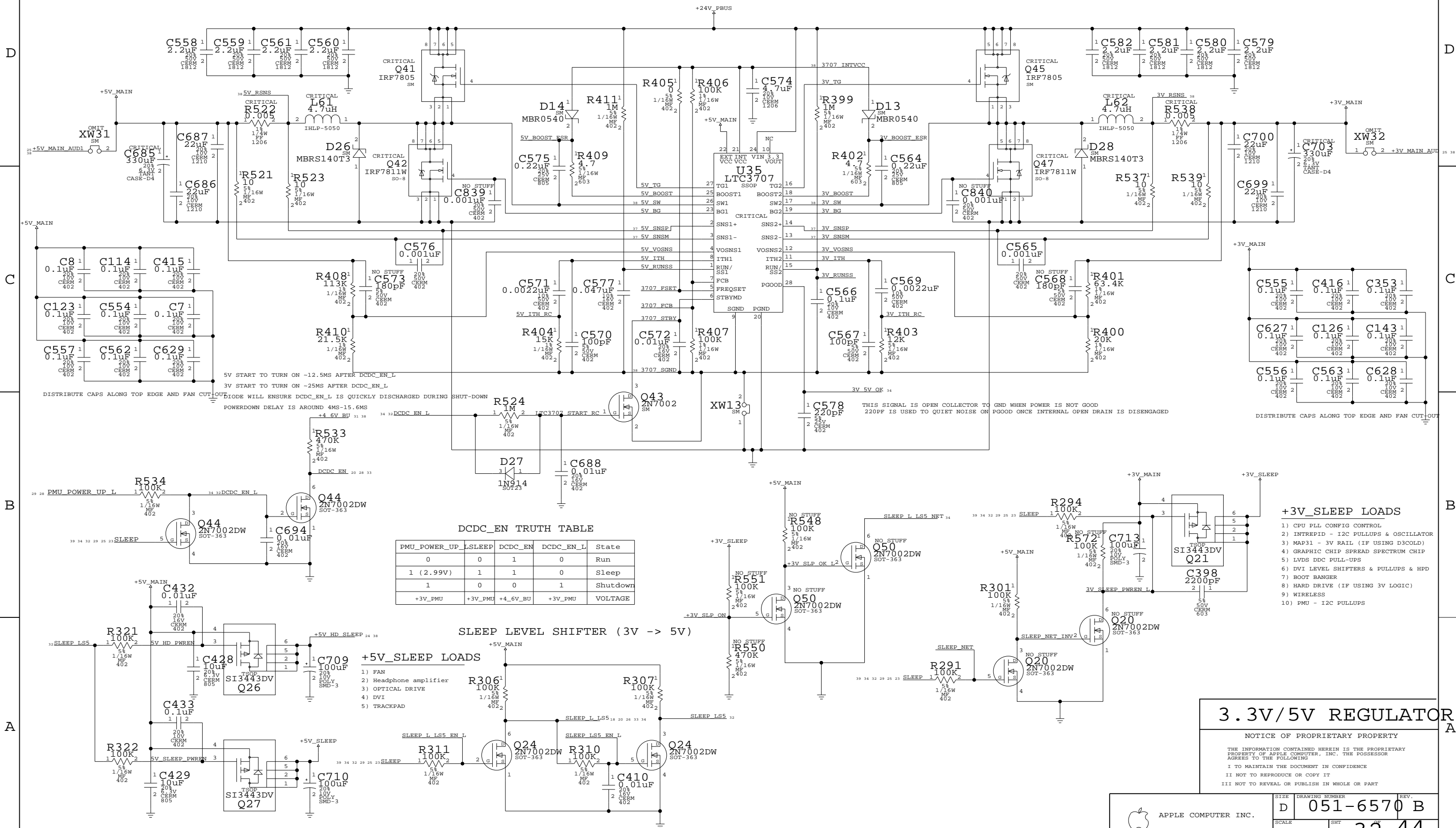
## BACKUP BATTERY

## 12.8V REGULATOR

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	NONE	31	44

# 3.3V/5V MAIN SUPPLY



DCDC_EN TRUTH TABLE				
PMU_POWER_UP	LSLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

- +3V\_SLEEP LOADS**
- 1) CPU PLL CONFIG CONTROL
  - 2) INTREPID - I2C PULLUPS & OSCILLATOR
  - 3) MAP31 - 3V RAIL (IF USING D3COLD)
  - 4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
  - 5) LVDS DDC PULL-UPS
  - 6) DVI LEVEL SHIFTERS & PULLUPS & HPD
  - 7) BOOT BANGER
  - 8) HARD DRIVE (IF USING 3V LOGIC)
  - 9) WIRELESS
  - 10) PMU - I2C PULLUPS

## 3.3V/5V REGULATOR

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# 1.5V/2.5V SWITCHER

## +1.5V\_SLEEP LOADS

- 1) AGP I/O - IF USING D3COLD
- 2) MAXBUS I/O - IF 1.5V INTERFACE

## +1.5V\_MAIN LOADS

- 1) INTREPID CORE

## +2.5V\_MAIN LOADS

- 1) MAP31 - FBCORE/FBIO IF USING D3HOT
- 2) GIGABIT ETHERNET - AVDDL
- 3) DDR SODIMMS - CORE/IO
- 4) DDR MUXES

## M11 Power Shut down Sequencing

## +2.5V\_SLEEP LOADS

- 1) FBCORE/FBIO IF USING D3COLD

# 1.8V SWITCHER

## +1.8V\_MAIN LOADS

- 1) INTREPID PLLS

## +1.8V\_SLEEP LOADS

- 1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
- 2) CPU JTAG & MaxBus Pull-ups
- 3) CPU PLL Config Straps

## 1.5V/1.8V/2.5V SUPPLIES

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[illegible]







# FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.  
FUNC\_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC\_QTY IS FOR REFERENCE AND  
LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.  
FUNC\_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
SCAN/TEST	JTAG ASIC TMS	TRUE		13 26
	JTAG ASIC TDI	TRUE		13
	JTAG ASIC TDO_TP	TRUE		26
	JTAG ASIC TCK	TRUE		13 26
	JTAG ASIC TRST L	TRUE		13 26
	CPU_CHKSTP_OUT L	TRUE		5
	CPU_SRESET L	TRUE		5
	CPU_HRESET L	TRUE		5 6 7
	JTAG_CPU_TMS	TRUE		5 6
	JTAG_CPU_TDI	TRUE		5 6
	JTAG_CPU_TDO_TP	TRUE		5
	JTAG_CPU_TCK	TRUE		5 6
	JTAG_CPU_TRST L	TRUE		5 6
	INT_JTAG_TDI	TRUE		13
	INT_TST_MONIN_PD	TRUE		13
	INT_TST_MONOUT_TP	TRUE		13
	INT_TST_PLLEN_PD	TRUE		13
	INT_I2C_CLK0	TRUE		6 11 13 23
	INT_I2C_DATA0	TRUE		6 11 13 23
	INT_I2C_CLK1	TRUE		13 14 25
INT I2C	INT_I2C_DATA1	TRUE		13 14 25
	+PBUS	TRUE		38
PWR/GND	+24V_PBUS	TRUE		38
	GPU_VCORE	TRUE		19 20 38
	1778_VFB	TRUE		20 38
	CPU_VCORE_SLEEP	TRUE		5 6 33 38
	VCORE_FB	TRUE		23 38
	+1.8V_MAIN	TRUE		38
	+2.5V_MAIN	TRUE		38
	+5V_MAIN	TRUE	2	38 39
	+5V_SLEEP	TRUE	2	38 39
	+3V_MAIN	TRUE	4	23 38
	+3V_PMU	TRUE		38
	CBUS_DET_1_L	TRUE		2000
CARDBUS DVI	CBUS_DET_2_L	TRUE		2000
	TMDS_DM<0..2>	TRUE		1000
	TMDS_DP<0..2>	TRUE		1000
	TMDS_CONN_CLKN	TRUE		1000
	TMDS_CONN_CLKP	TRUE		1000
	VGA_R	TRUE		1000
	VGA_G	TRUE		1000
	VGA_B	TRUE		1000
	VGA_HSYNC	TRUE		1000
	VGA_VSYNC	TRUE		1000
	DVI_DDC_CLK_UF	TRUE		1000
	DVI_DDC_DATA_UF	TRUE		1000
LVDS	DVI_HPD_UF	TRUE		1000
	+5V_DDC_SLEEP	TRUE		2000
	CHGND1	TRUE	2	2000
	CHGND1	TRUE	6	1000
	LVDS_L0N	TRUE		1000
	LVDS_L0P	TRUE		1000
	LVDS_L1N	TRUE		1000
	LVDS_L1P	TRUE		1000
	LVDS_L2N	TRUE		1000
	LVDS_L2P	TRUE		1000
	CLKLVDS_LN	TRUE		1000
	CLKLVDS_LP	TRUE		1000
INVERTER	LVDS_DDC_CLK	TRUE		1000
	LVDS_DDC_DATA	TRUE		1000
	+3V_LCD	TRUE	2	2000
	+3V_SLEEP	TRUE		2000
	CHGND4	TRUE	2	2000
	CHGND4	TRUE	6	1000
	+14V_INV	TRUE		2000
	+5V_INV_SW	TRUE		2000
	BRIGHT_PWM	TRUE		2000
	INV_GND	TRUE		2000
	TV_C	TRUE		2000
	TV_Y	TRUE		2000
S-VIDEO	TV_COMP	TRUE		2000
	TV_GND1	TRUE		2000
	TV_GND2	TRUE		2000
	INT_I2S0_SND_TO_DAC	TRUE		1000
	INT_I2S0_SND_LRCLK	TRUE		1000
	INT_I2S0_SND_MCLK	TRUE		1000
	INT_I2S0_SND_SCLK	TRUE		1000
	INT_I2S0_SND_FROM_ADC	TRUE		1000
	SND_HP_MUTE_L	TRUE		1000
	SND_HP_MUTE	TRUE		1000
	SND_HW_RESET_L	TRUE		1000
	SND_HP_SENSE_L	TRUE		1000
LIO	SND_LIN_SENSE_L	TRUE		1000
	INT_I2C_CLK2	TRUE		1000
	INT_I2C_DATA2	TRUE		1000
	ADAPTER_DET	TRUE		1000
	CHARGE_LED_L	TRUE		1000
	NEC_LUSB_OCI_UF	TRUE		1000
	NEC_LUSB_PPON	TRUE		1000
	+5V_MAIN	TRUE	2	2000
	+5V_SLEEP	TRUE	2	2000
	+3V_SLEEP	TRUE		2000
	+3V_SLEEP	TRUE		2000

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
USB	NEC_USB_DAM	TRUE		17 25 37
	NEC_USB_DAP	TRUE		17 25 37
	NEC_USB_DBM	TRUE		17 25 37
	NEC_USB_DBP	TRUE		17 25 37
	BT_USB_DM	TRUE		14 25 37
	BT_USB_DP	TRUE		14 25 37
	MODEM_USB_DM	TRUE		14 25 37
	MODEM_USB_DP	TRUE		14 25 37
	NEC_RUSB_PPON	TRUE		17 25
	NEC_RUSB_OCI_UF	TRUE		17 25
	PCI_AD<0..31>	TRUE		1000
	PCI_FRAME_L	TRUE		1000
	PCI_TRDY_L	TRUE		1000
	PCI_IRDY_L	TRUE		1000
	PCI_DEVSEL_L	TRUE		1000
	PCI_STOP_L	TRUE		1000
	PCI_PAR	TRUE		1000
	AIRPORT_PCI_REQ_L	TRUE		1000
	AIRPORT_PCI_GNT_L	TRUE		1000
	AIRPORT_PCI_INT_L	TRUE		1000
RT. USB WIRELESS	MAIN_RESET_L	TRUE		1000
	CLK33M_AIRPORT	TRUE		1000
	PMU_PME_L	TRUE		1000
	ROM_ONBOARD_CS_L	TRUE		1000
	ROM_OE_L	TRUE		1000
	ROM_CS_L	TRUE		1000
	ROM_RW_L	TRUE		1000
	RF_DISABLE_L	TRUE		1000
	AIRPORT_CLKRUN_L	TRUE		1000
	+3V_AIRPORT	TRUE		1000
	CHGND3	TRUE	6	1000
OPTICAL	EIDE_OPTICAL_DATA<0..15>	TRUE		2000
	EIDE_OPTICAL_DMA_RQ	TRUE		2000
	EIDE_OPTICAL_READ_L	TRUE		2000
	EIDE_OPTICAL_DMAACK_L	TRUE		2000
	EIDE_OPTICAL_ADDR<0..2>	TRUE		2000
	EIDE_OPTICAL_CS0_L	TRUE		2000
	EIDE_OPTICAL_CS1_L	TRUE		2000
	EIDE_OPTICAL_RST_L	TRUE		2000
	EIDE_OPTICAL_WR_L	TRUE		2000
	EIDE_OPTICAL_IOCHRDY	TRUE		2000
	EIDE_OPTICAL_INT	TRUE		2000
TRACKPAD	+5V_TPAP_SLEEP	TRUE		3000
	TPAD_F_TXD	TRUE		3000
	TPAD_F_RXD	TRUE		3000
	LID_CLOSED_L	TRUE		3000
	+3V_HALL_EFFECT	TRUE		3000
	SOFT_PWR_ON_L	TRUE		3000
	COMM_RESET_L	TRUE		4000
	COMM_SHUTDOWN	TRUE		4000
	COMM_RING_DET_L	TRUE		4000
	COMM_TXD_L	TRUE		4000
MODEM/ SERIAL	COMM_TRXC	TRUE		4000
	COMM_GPIO_L	TRUE		4000
	COMM_DTR_L	TRUE		4000
	COMM_RTS_L	TRUE		4000
	COMM_RXD	TRUE		4000
KEYBOARD	KBD_ID	TRUE		3000
	KBD_INTL	TRUE		3000
	KBD_JIS	TRUE		3000
	KBD_CAPSLOCK_LED	TRUE		3000
	KBD_NUMLOCK_LED	TRUE		3000
	KBD_FUNCTION_L	TRUE		3000
	KBD_COMMAND_L	TRUE		3000
	KBD_OPTION_L	TRUE		3000
	KBD_CONTROL_L	TRUE		3000
	KBD_SHIFT_L	TRUE		3000
BATTERY	KBD_X<0..9>	TRUE		3000
	KBD_Y<0..7>	TRUE		3000
	+BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000
	BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000
	BATT_CLK	TRUE		1000
	BATT_DATA	TRUE		1000
	PMU_BATT_DET_L	TRUE		1000
FANS	+FAN_PWR	TRUE		3000
	FAN1_TACH	TRUE		3000
	FAN2_TACH	TRUE		3000
	FAN1_GND	TRUE		3000
	FAN2_GND	TRUE		3000
ETHERNET	MDI_P<0..3>	TRUE		1000
	MDI_M<0..3>	TRUE		1000
FIREWIRE	FW_TP00P	TRUE		1000
	FW_TP00N	TRUE		1000
	FW_TP00R	TRUE		1000
	FW_TP10P	TRUE		1000
	FW_TP10N	TRUE		1000
	+FW_VP0	TRUE		1000
	FW_VGND	TRUE		1000

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
FIREWIRE (CONT.)	FW_TP01P	TRUE		1000
	FW_TP01N	TRUE		1000
	FW_TP11P	TRUE		1000
	FW_TP11N	TRUE		1000
	+FW_VP1	TRUE		1000
	FW_VGND	TRUE		1000
DC PWR IN	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000
LMU/ALS	ST7_SLEEP_LED_H	TRUE		23
	PMU_SLEEP_LED	TRUE		23
	PMU_LID_CLOSED_L	TRUE		23 29
	LMU_DETECT	TRUE		23
MISC.	CHGND2	TRUE	6	1000
	(100 MIL PROBE PREFERRED)			23
	SLEEP_LED	TRUE		23
	PMU_KB_RESET_L	TRUE		29
	SLEEP	TRUE		23 25 29 32 34
	PMU_CPU_HRESET_L	TRUE		6 29
	BB_RESET_L	TRUE		6
	+3V_PMU_RESET	TRUE		29 33
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SCALE		NONE	SHT	39 OF 44

	8	7	6	5	4	3	2	1
	REVISION HISTORY							
	Proto/EVT Release							
	10/27/03 - 1. Schematic originated from Q16 MLB							
D	11/10/03 - 1. Replace U56 symbol 2. Connect OVDDSENSE to MAXBUS_SLEEP 3. Modify SRWD, SRW1 and IABTRY0 connection 4. Connect VDD (page 6) to CPU_VCORE_SLEEP (PAGE 5) 5. Connect SENSEVDD to CPU_VCORE_SLEEP 6. Connect SENSEGND to GND 7. Add 4 pos 0 ohm resistor for AMD BootRom issue (R1,R194,R236,R271) 8. Connect TEMP_ANODE and TEMP_CATHODE to ADT7460 9. Modify CPU PLL config 10. Add 0 ohm resistor on CG_FSEL Interpid side(R450) 11. Replace U47 symbol 12. Change R743 from 2m ohm to 1m ohm 13. Change R774, C781, C788, C793, C797, C802 from 220uF to 330uF 14. Change R748 from 410 ohm to 10 ohm							
	12/01/03 - 1. Modify CPU_VCORE setting.							
	12/02/03 - 1. Modify CPU_BTR CPU_VCORE VID setting							
	12/05/03 - 1. Add CPU AVDD LDO (Page 5) 2. Change Q45 and Q41 to IRE7805 (376S0035) 3. Change Q47 and Q42 to IRE7811W (376S0104) 4. Change R402 and R409 to 4.7ohm resistors 5. Connect INT_TDO from Intrepid to Cypress Chip PD* (U31)							
	12/12/03 - 1. Add R468 and R601 for MAX1715 2.5V adjust 2. Modify CPU_VCORE setting to Motorola new spec 3. Modify LDO power sequence							
	12/16/03 - 1. Add 10K pull down for INT_TDO on page 13							
	12/17/03 - 1. Change LDO Vin from +3V_MAIN to +3V_SLEEP 2. Connect INT_TDO from Intrepid to Marvell 88E1111(U43) 3. Add R755,R756,R758,R759 for power rail							
	DVT Release (Rev. 02)							
	01/30/04 - 1. Add Soft Modem(Pin#14) 10K pull-up at J15.7 (Pg 25) 2. Add Bom Table for R97 2.21K ohm VCore Offset (Pg 33)							
	02/04/04 - 1. C811 change to 4.7uF per MOT A7PM requirement (Pg 5) 2. NO STUFF R236,R1,R271&R194 to remove PCI stub (Pg 9)							
	DVT Release (Rev. 03)							
	02/12/04 - 1. CPU VCore adjustment for V1.1 A7PM CPU (Pg 33) 2. CPU AVDD adjustment for V1.1 A7PM CPU (Pg 5) 3. Add INT_TMDS termination change to 0 ohm Qty:8 (Pg 20) 4. Add I/O VREF Voltage divider change to both 1K ohm (Pg 12)							
	DVT Release (Rev. 04)							
	02/13/04 - 1. INT. TMDS Termination change to 2* 49.9ohm = 100ohm (Pg 20)							
	PVT Release (Rev. A)							
C	03/11/04 - 1. INT. TMDS Termination change to 2* 75 ohm = 150ohm (except CLK pair) (Pg 20) 2. USB series termination near NEC PHY change to 47 ohm (Pg 17)							
	PVT Release (Rev. A)							
	04/02/04 - 1. USB series termination near NEC PHY change to 43.2 ohm (Pg 17)							


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